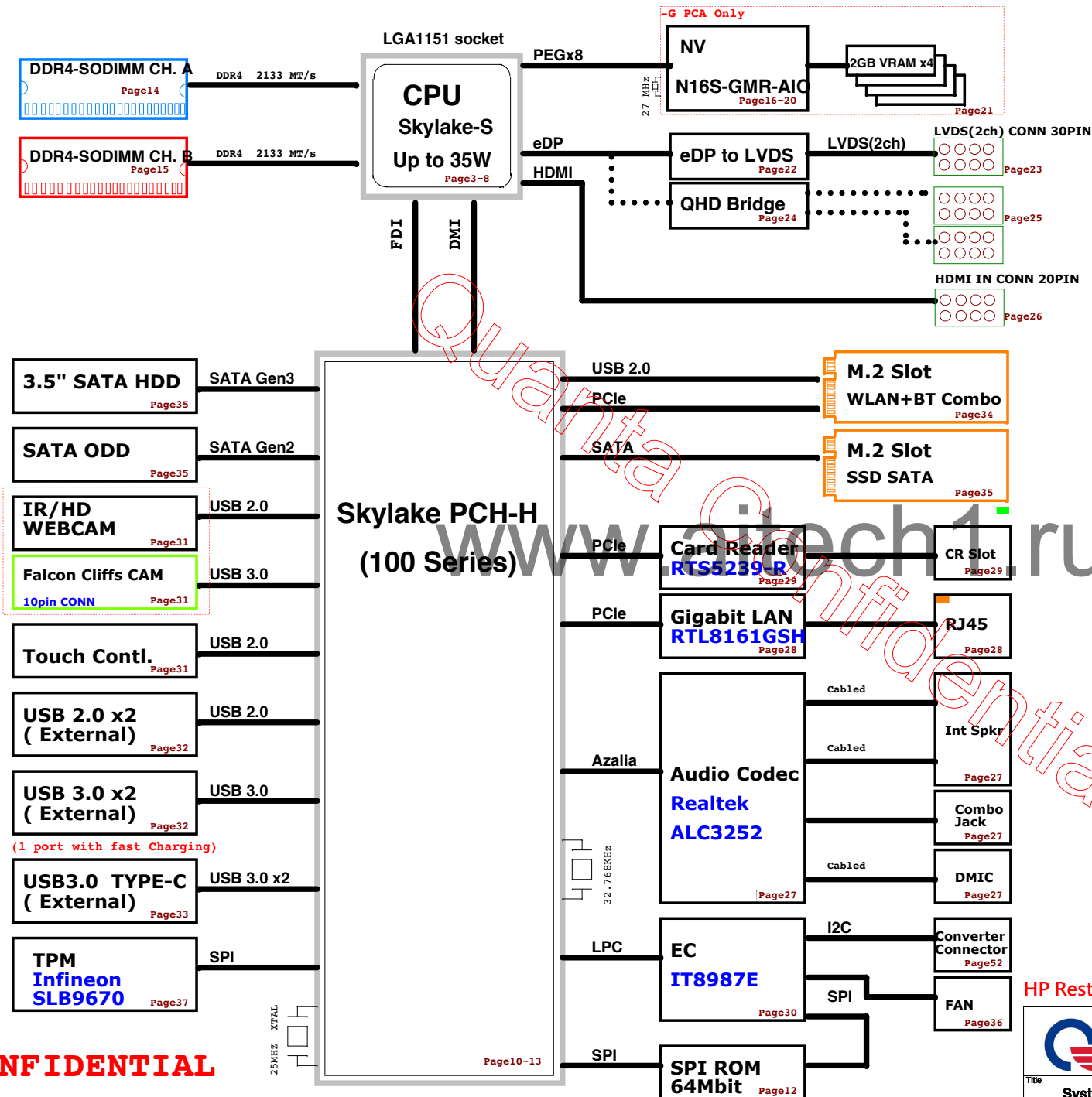


# HP Saipan System Block Diagram

01



CONFIDENTIAL

HP Restricted Secret



Quanta Computer Inc.

Project: HP-Saipan

Title			System Block Diagram
Size	Document Number	Rev	A
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## Voltage Rails

02

Power Rail	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal
+RTC_VCC	3V	ON	ON	ON	ON	ON	ON	
+VIN	19V	ON	ON	ON	ON	ON	ON	Adapter in
+5V_ALW	5V	ON	ON	ON	ON	ON	ON	Int. LDO
+3V_ALW	3.3V	ON	ON	ON	ON	ON	ON	Int. LDO
+3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	LDO
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_ON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_ON
+1.8V_S5	1.8V	ON	ON	ON	ON	OFF	OFF	S5_ON
+1V_S5	1.0V	ON	ON	ON	ON	OFF	OFF	PG_+1.8V_S5
+VCCST_VCCPLL	1.0V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
+VDDQ	1.35V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	DDR_VTT_CNTL
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+3V	3V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+VCCIO	0.95V	ON	OFF	OFF	OFF	OFF	OFF	PG_MAIN
+VCCSA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+VCCIO
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON
+3.3V_VGA	3.3V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA
+1.05V_VGA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN
+VGA_CORE	0.8~1.15V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN
+1.35V_VGA	1.35V	ON	OFF	OFF	OFF	OFF	OFF	EN_+1.35V_VGA
+VCCCORE	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON

RTC Batt, PCH , EC

LED

EC

System

PCH, USB, 3D WebCAM, Touch Panel, USB Charger

PCH, XDP, SPI flash ROM,NGFF LAN

PCH, XDP, NGFF LAN

PCH

CPU, PCH, XDP

DDR4, CPU DDR4 I/O

DDR4

HDD, ODD,Audio AMP,Panel VCC,FAN

PCH, Audio, Card Reader, TPM, FHD CAM

3.5" HDD

CPU

CPU

CPU

dGPU

dCPU

dGPU

dGPU, VRAM

CPU

## Schematic "Value" Definition

Intel Platform Saipan-G and Saipan-U			DB/SI/PV Stage		MP		ALL STAGE	
By Value format	Description	Auto BOM Control	UMA	Discrete N16S GPU	UMA	Discrete N16S GPU	QHD PANEL	FHD PANEL
XX	Install	V	V	V	V	V		
*XX	Non-Install	V						
PROTO@XX	Install in Pre-production only	V	V	V				
MP@XX	Install in MP only	V			V	V		
DIS@xx	Install Discrete (DGPU) only	V		V		V		
UMA@xx	Install UMA	V	V		V			
QHD@xx	QHD panel	V	V	V	V	V	V	
FHD@xx	FHD panel	V	V	V	V	V		V

\*\*\*Board ID and VRAM ID by manual control

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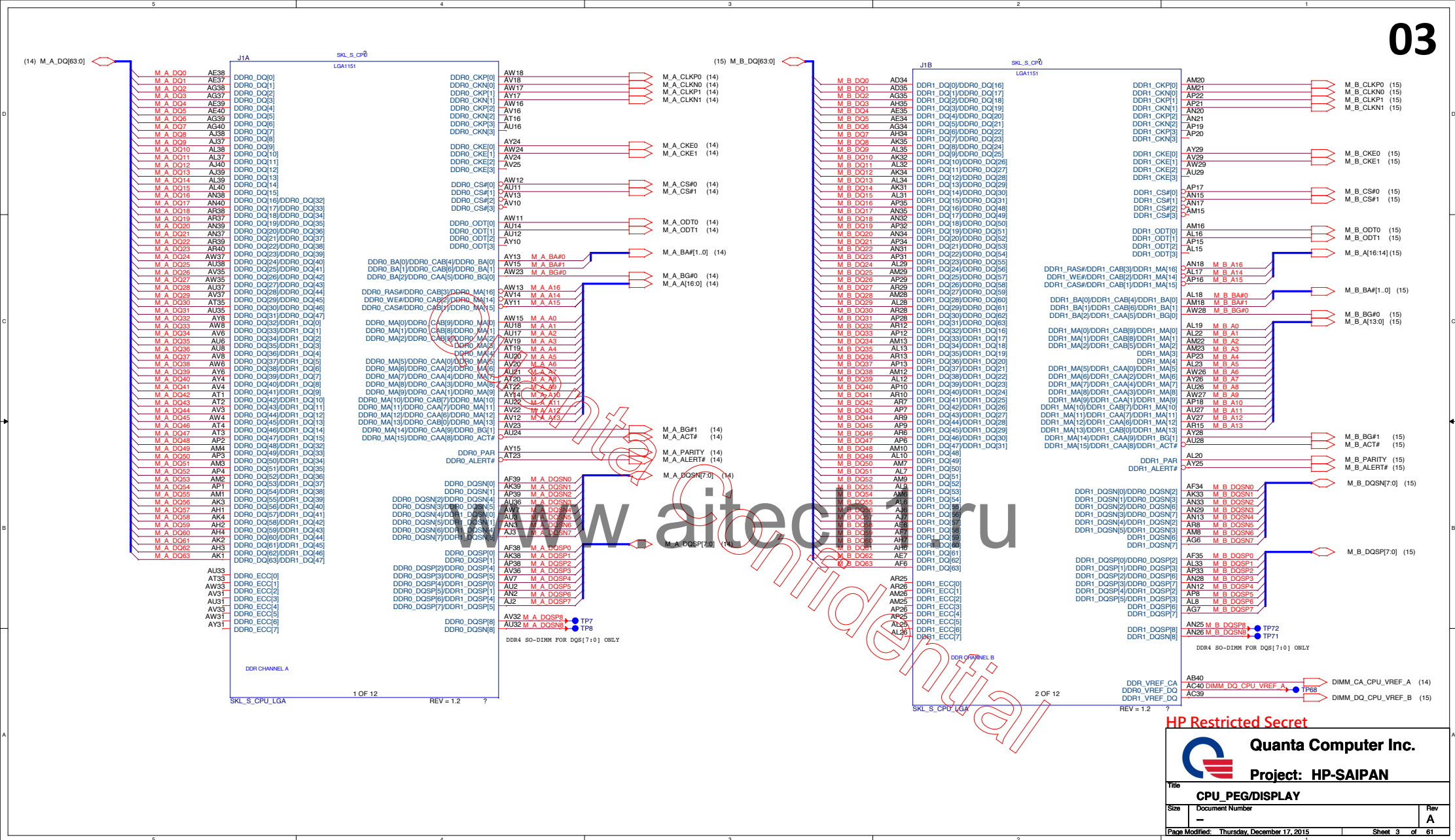


Quanta Computer Inc.

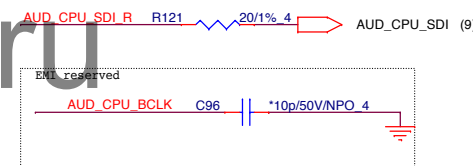
Project: HP-Saipan

Title			Power States & Value Definition
Size	Document Number	Rev	A
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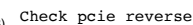






Title		
CPU_PEG/DISPLAY		
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EC-DB-E02

EC-DB-E03

H_TCK	TERMINATION	PLACE	NEAR	CPU	WITHIN
1.1	INCH				

**BK: FOLLOW CRB 1.1**

PD TEST	CPU	R492	~1K 4
PD TEST CPU 1	R484	~1K 4	
PD TEST CPU 2	R489	~1K 4	
PD TEST CPU 3	R496	~1K 4	
PD TEST CPU 4	R517	~1K 4	
PD TEST CPU 5	R513	~1K 4	
PD TEST CPU 6	R514	~1K 4	
PD TEST CPU 7	R515	~1K 4	
PD TEST CPU 8	R488	~1K 4	
PD TEST CPU 9	R487	~1K 4	
PD TEST CPU 10	R494	~1K 4	
PD TEST CPU 11	R495	~1K 4	
PD TEST CPU 12	R518	~1K 4	
PD TEST CPU 13	R519	~1K 4	
PD TEST CPU 14	R526	~1K 4	
PD TEST CPU 15	R523	~1K 4	

Unstuff R461 & R462 for SPT-H

+3V\_S5

SKL CNL R6 \*10k/5% 4

SKL PCUSTB 0 DP	R483	*1K 4
SKL PCUSTB 0 DN	R481	*1K 4
SKL PCUSTB 1 DP	R499	*1K 4
SKL PCUSTB 1 DN	R503	*1K 4

BK: CRB --> NO THESE , NEED CONFIRM

+VCCST VCCPLI

CRB: Close to SPT-H

H\_PWRGD R564 \*10k/5%\_4



EC-DB2-E01

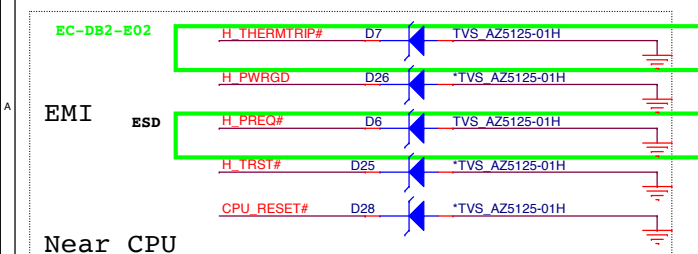
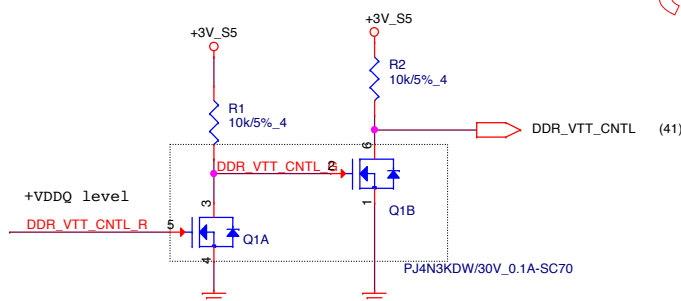
R552 SP 4

R559 \*0/5% 4

EC\_PECI

PCH\_PECI

## DDR VTT CNTL



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**Quanta Computer Inc.****Project: HP-SAIPAN**

Title **CPU MISC**

Size	Document Number
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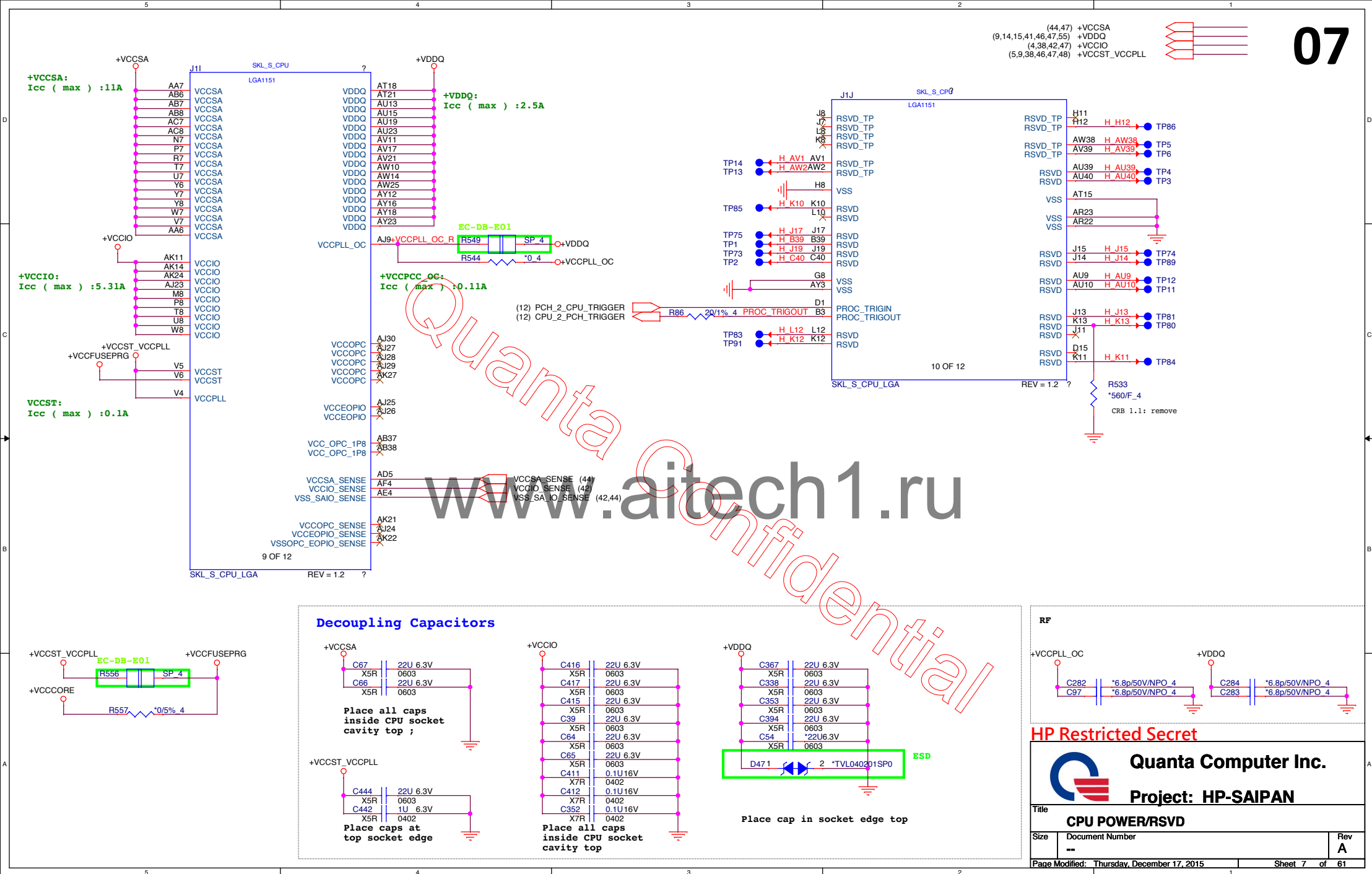
Page Modified: Thursday, December 17, 2015

Rev	
A	

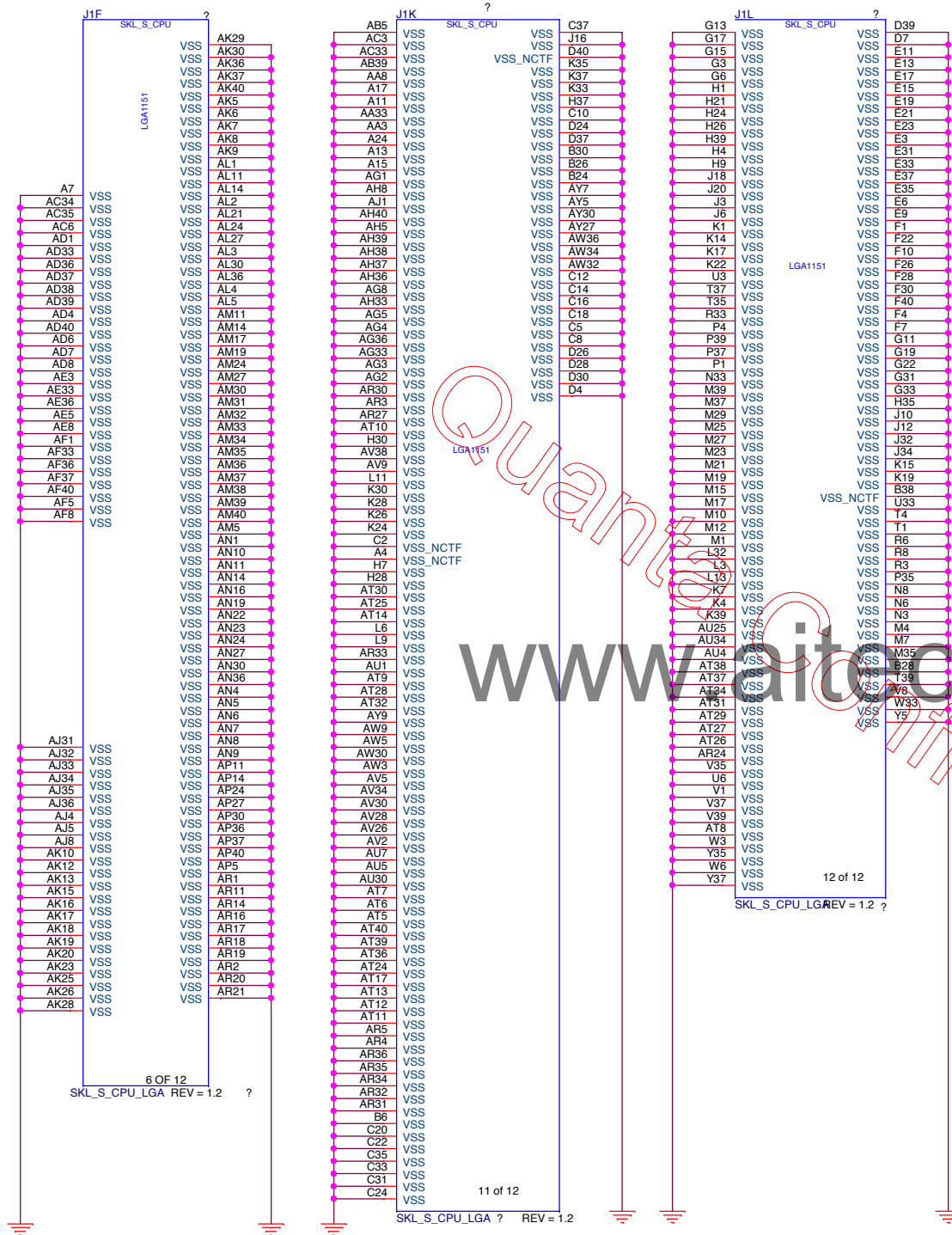












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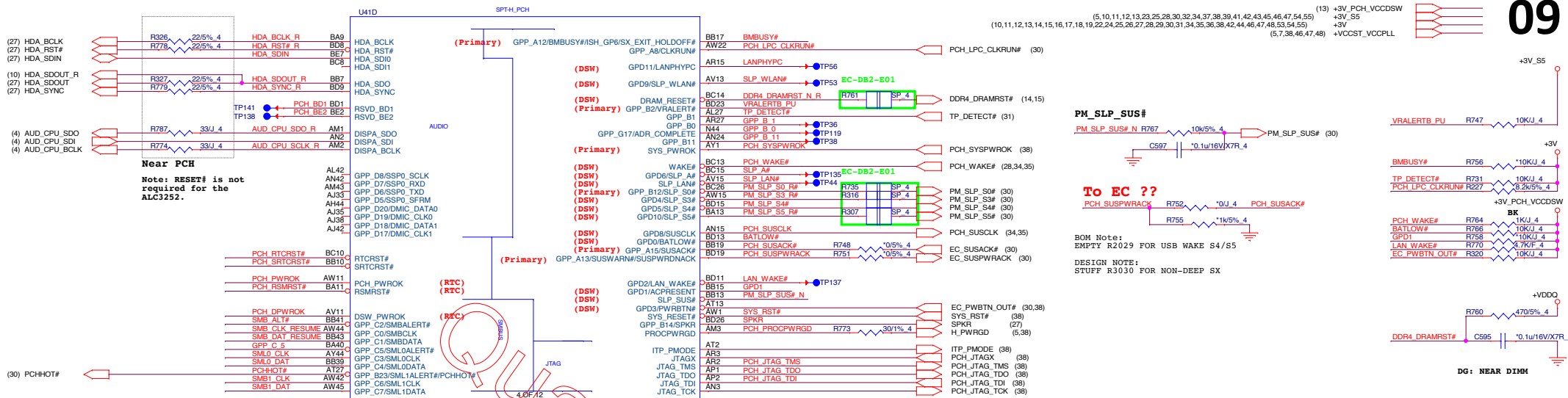


Quanta Computer Inc.

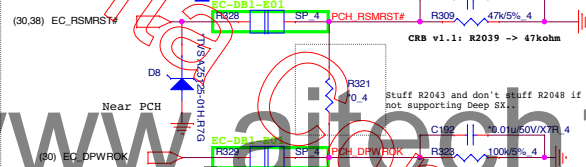
Project: HP-SAIPAN

Title		
CPU GND		
Size	Document Number	Rev
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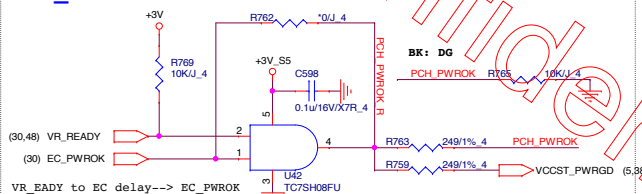




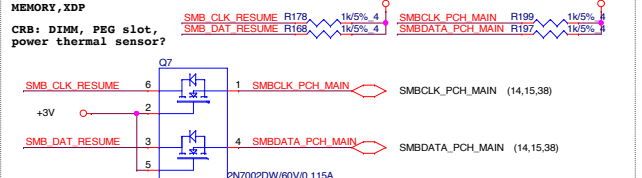
## RSMRST# &amp; DSW PWROK



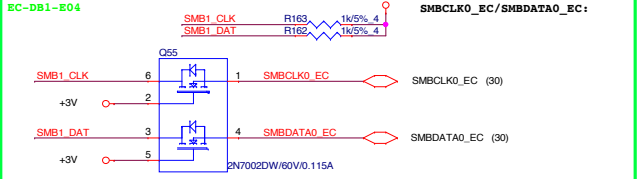
## PCH\_PWROK



## SYSTEM SMBUS

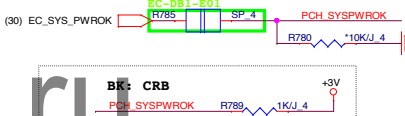


## SYSTEM SMBUS

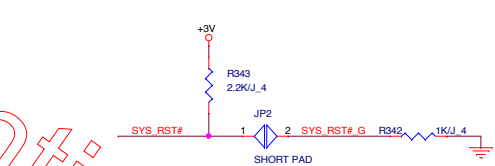


## PCH\_SYSPWROK

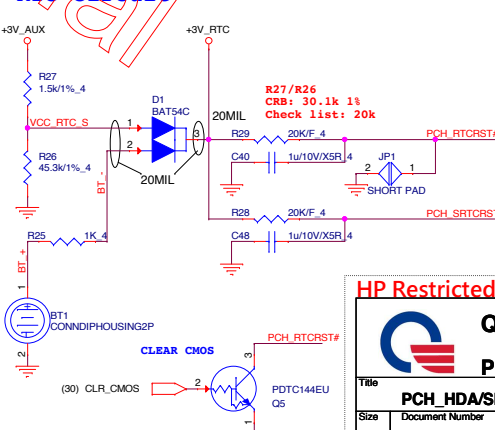
(Be asserted after both PWROK and VR\_READY assertion)



## PCH SYSTEM RESET



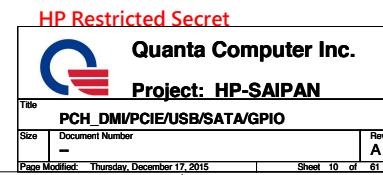
## RTC circuit



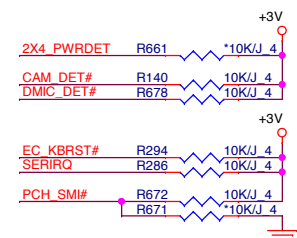
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Quanta Computer Inc.	
Project: HP-SAIPAN	
Title	PCH_HDA/SMBUS/MISC
Size	Document Number
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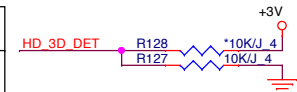






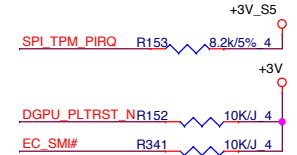


3D camera	1
HD camera	0



CRB: Connect to +3V\_S5 directly

**SERIRQ & LPC\_PIRQ**  
Note: An external pull-up is required



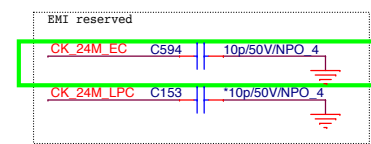
```

H/W STRAPS:
DDPB_CTRLDATA: ( pull up at HDMI page )
0= Port B is not detected. Default, Internal PD
1= Port B is detected.

```

```
DGPU_HOLD_RST#
0 = Keep dGPU in reset
1 = Reset is released. This action taken 100 ms after
DGPU_PWROK to ensure clock is stable.
```

EN\_DGPU\_PWR  
1 = dGPU power switch turned on  
0 = Power switch turned off



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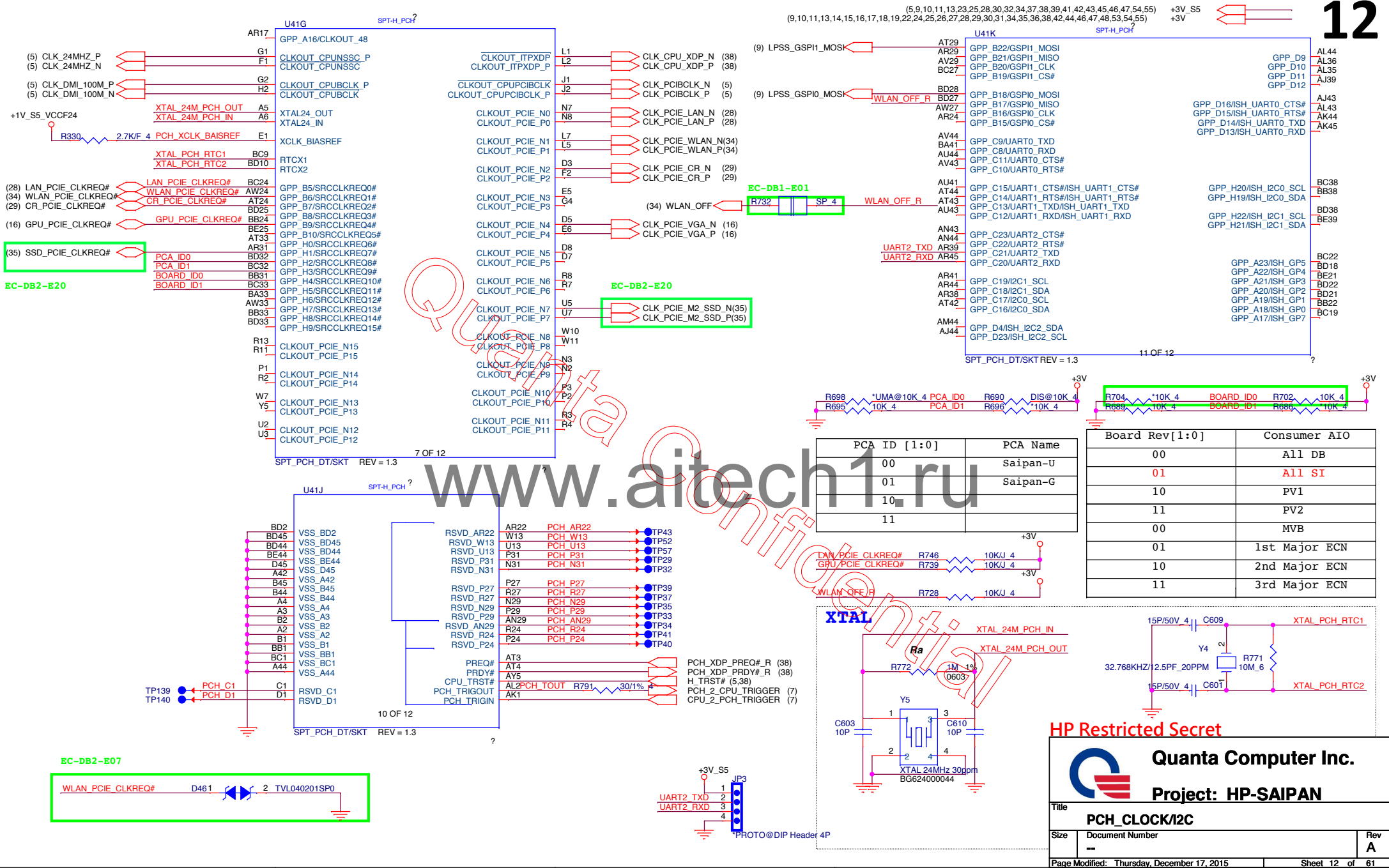


**Quanta Computer Inc.**

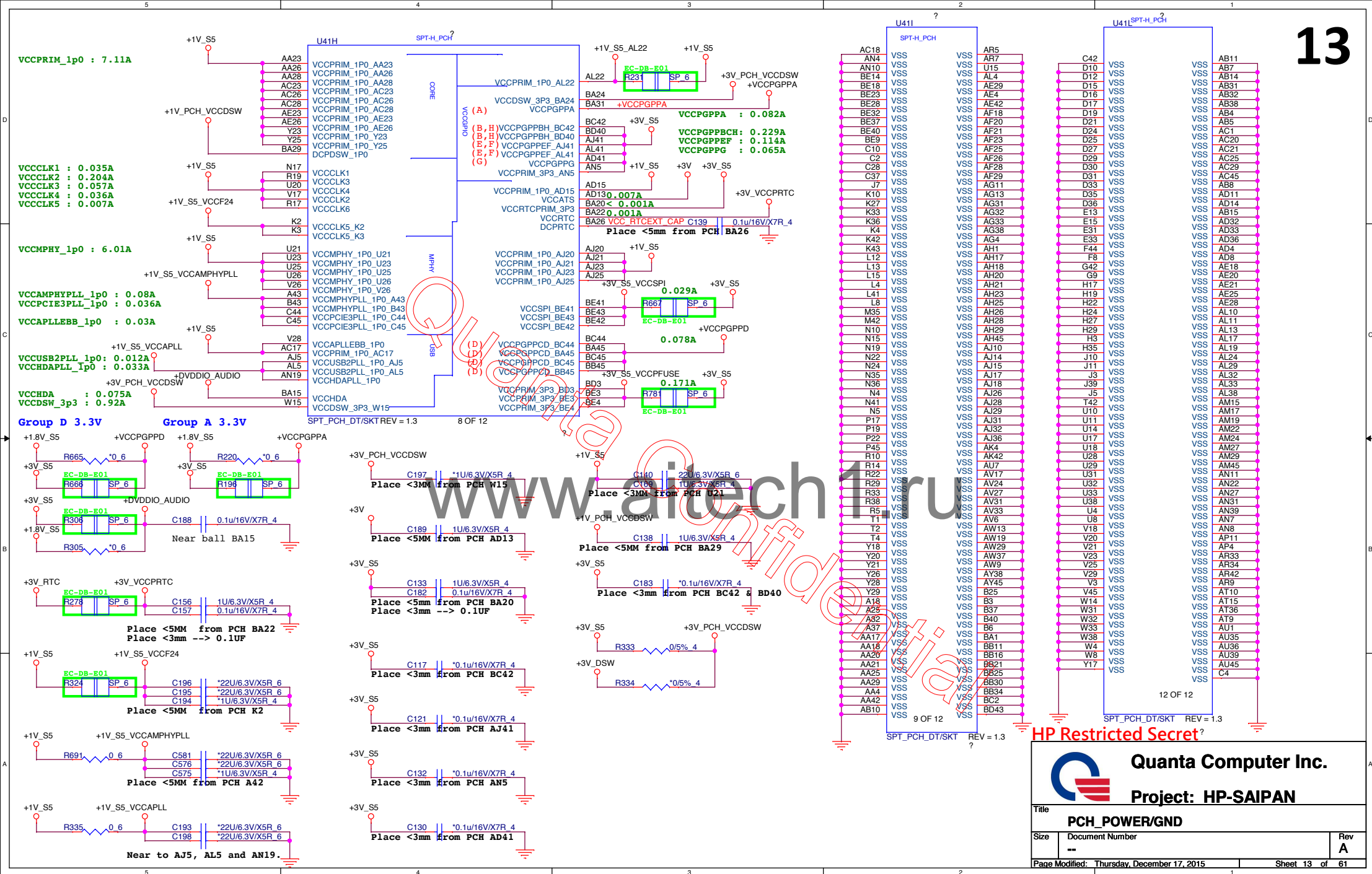
**Project: HP-SAIPAN**

Title <b>PCH_USB3/LPC</b>			Rev <b>A</b>
Size	Document Number <b>---</b>		
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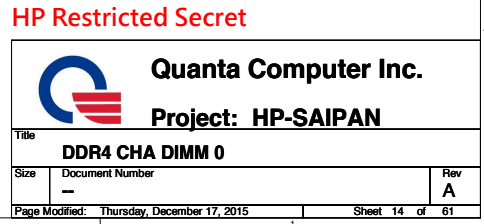
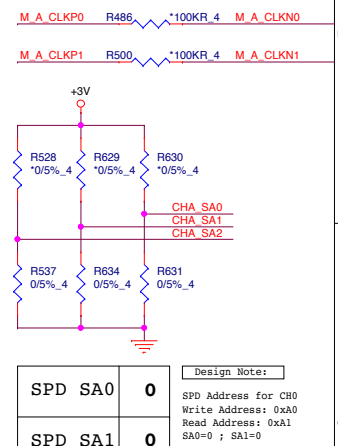




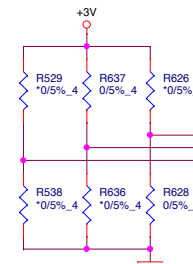
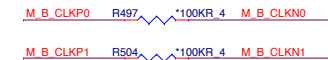




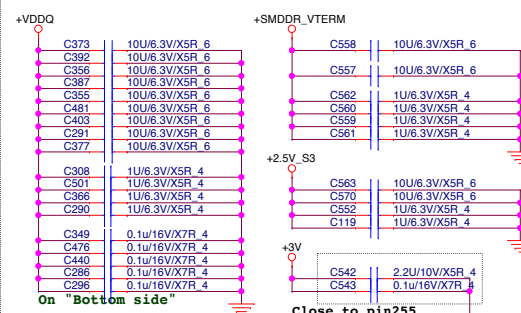








SPD SA0	0
SPD SA1	1



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**Quanta Computer Inc.**

**Project: HP-SAIPAN**

Title  
**DDR4 CHB DIMM 1**

Size	Document Number
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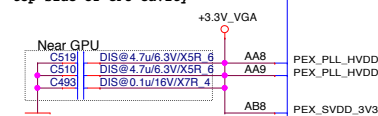
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[illegible]

Place all above caps on  
top side of CPU cavity



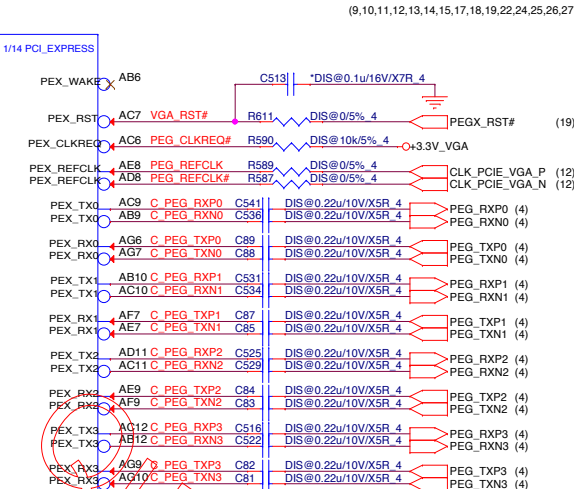
(53) VGA\_VDD\_SEN      F2      VDD\_SENSE

(53) VGA\_GND\_SEN      F1      GND\_SENSE

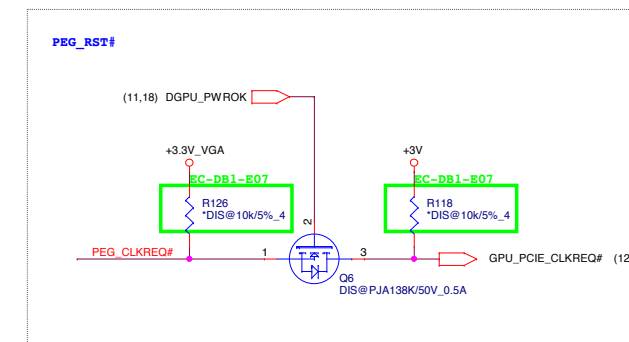
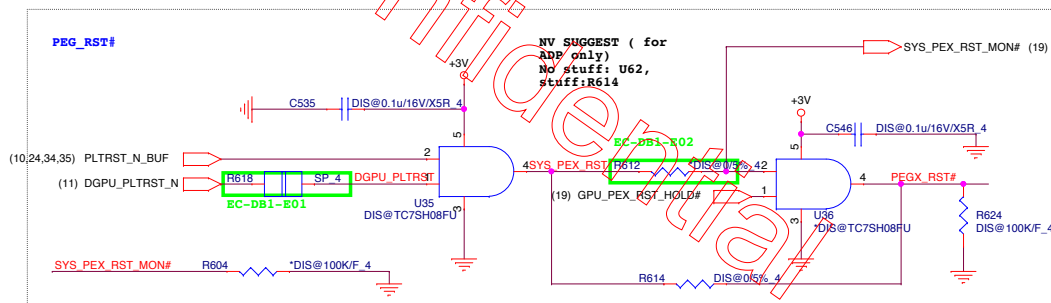
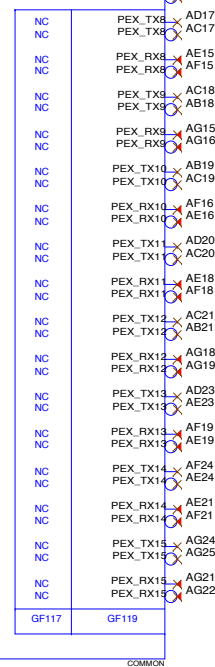
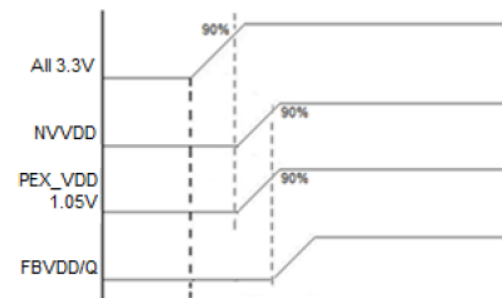
Timing diagram showing various signals and their transitions:

- R527**: Signal transition at approximately 10ns.
- DIS@200/1%**: Signal transition at approximately 10ns.
- PEX\_TSTCLK**: Signal transition at approximately 10ns.
- AF22**: Signal transition at approximately 10ns.
- PEX\_TSTCLK\_OUT**: Signal transition at approximately 10ns.
- PEX\_TSTCLKF**: Signal transition at approximately 10ns.
- AE22**: Signal transition at approximately 10ns.
- CX300T30001 Change to 0ohm**: Signal transition at approximately 10ns.
- DIS@0.5%**: Signal transition at approximately 10ns.
- DIS@4.7u/6.3V/X5R.6**: Signal transition at approximately 10ns.
- PEX\_PLLVDD**: Signal transition at approximately 10ns.
- AA14**: Signal transition at approximately 10ns.
- AA15**: Signal transition at approximately 10ns.
- PEX\_PLLVDD**: Signal transition at approximately 10ns.
- DIS@0.1u/6.3V/X5R.4**: Signal transition at approximately 10ns.
- DIS@0.1u/16V/X7R.4**: Signal transition at approximately 10ns.
- R579**: Signal transition at approximately 10ns.
- DIS@10k/5%**: Signal transition at approximately 10ns.
- TESTMODE**: Signal transition at approximately 10ns.
- AD9**: Signal transition at approximately 10ns.
- TESTMODE**: Signal transition at approximately 10ns.
- R49**: Signal transition at approximately 10ns.
- DIS@2.49k/1%**: Signal transition at approximately 10ns.
- PEX\_TERM**: Signal transition at approximately 10ns.
- AF25**: Signal transition at approximately 10ns.
- PEX\_TERM**: Signal transition at approximately 10ns.

see 595-modle n13p22-522

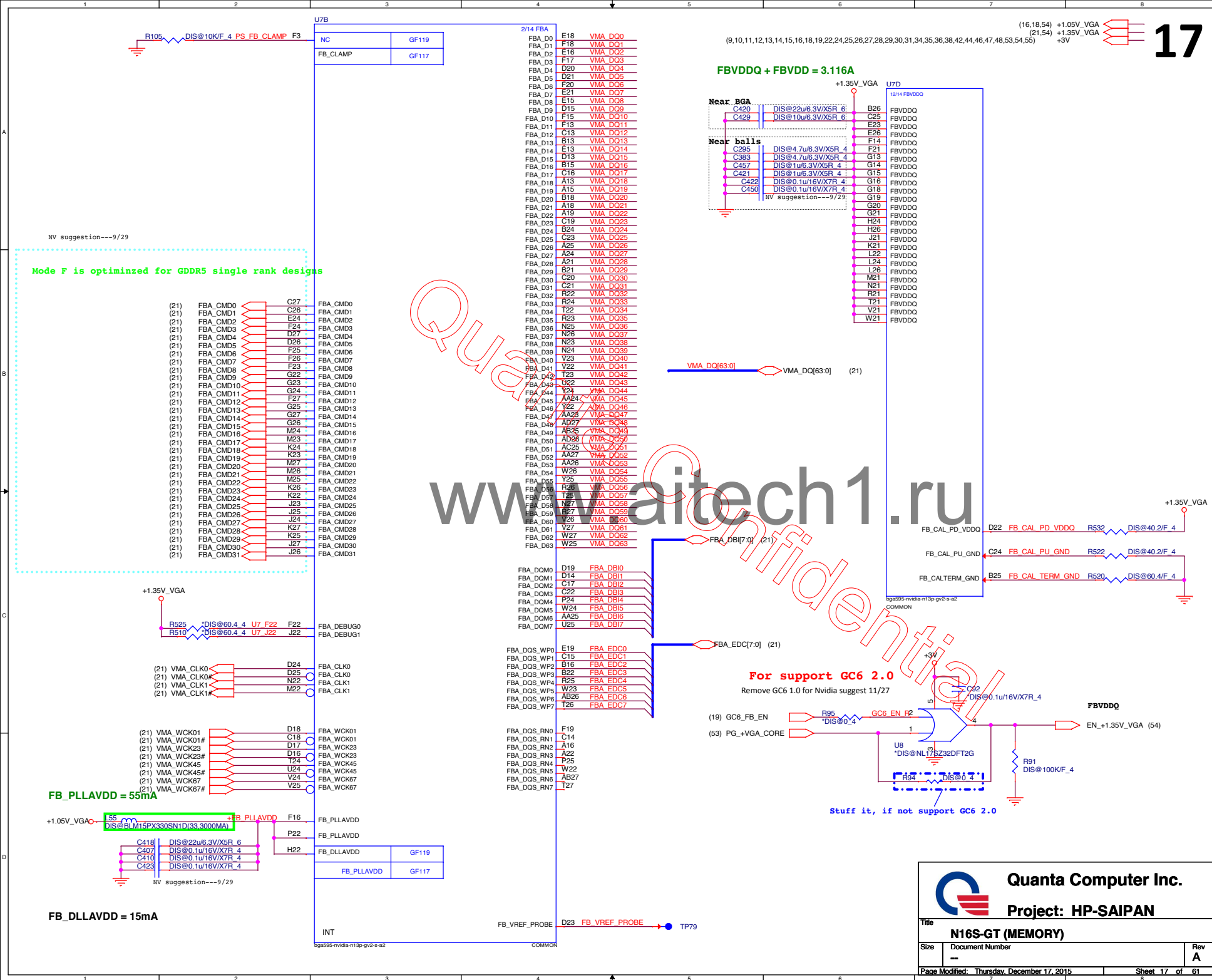


```
swap pin for layout
```

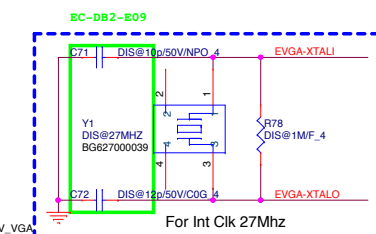


16

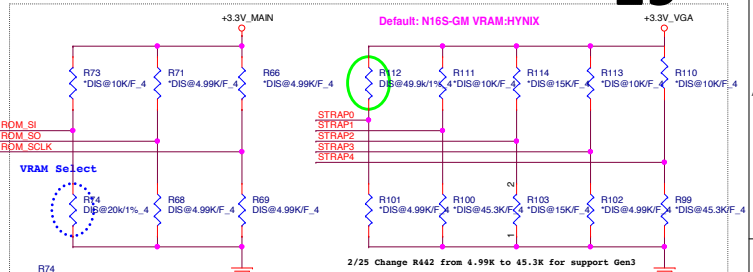
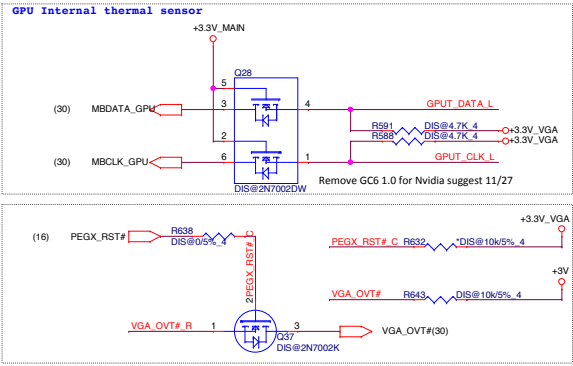
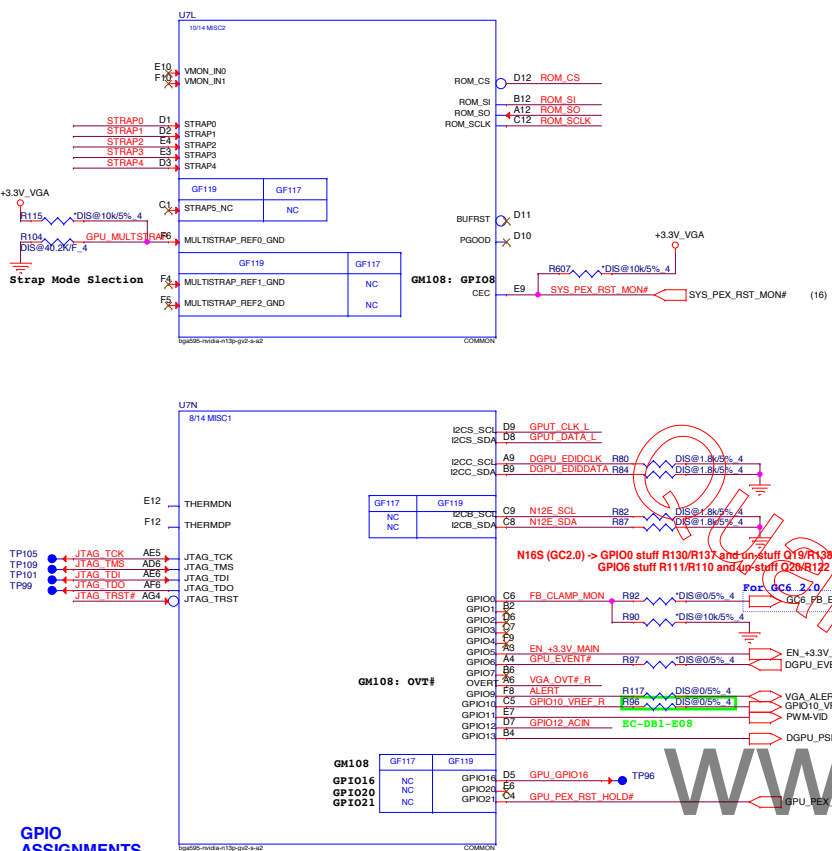














**Project: HP-SAIPAN**

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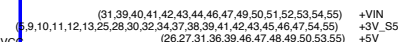




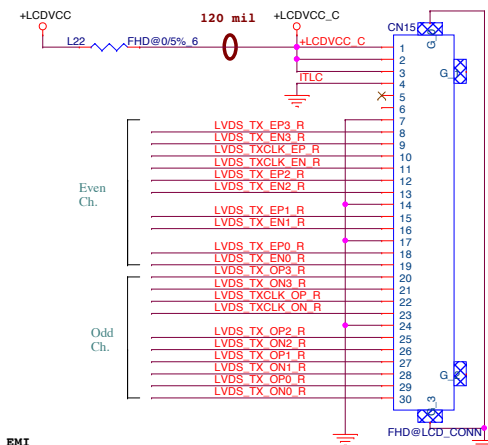




## 23



## LVDS Conn



## EMI



Close to CN18

**Project: HP-SAIPAN**

Panel (Control).LCD-Conn.

Size

Size	Document Number
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100

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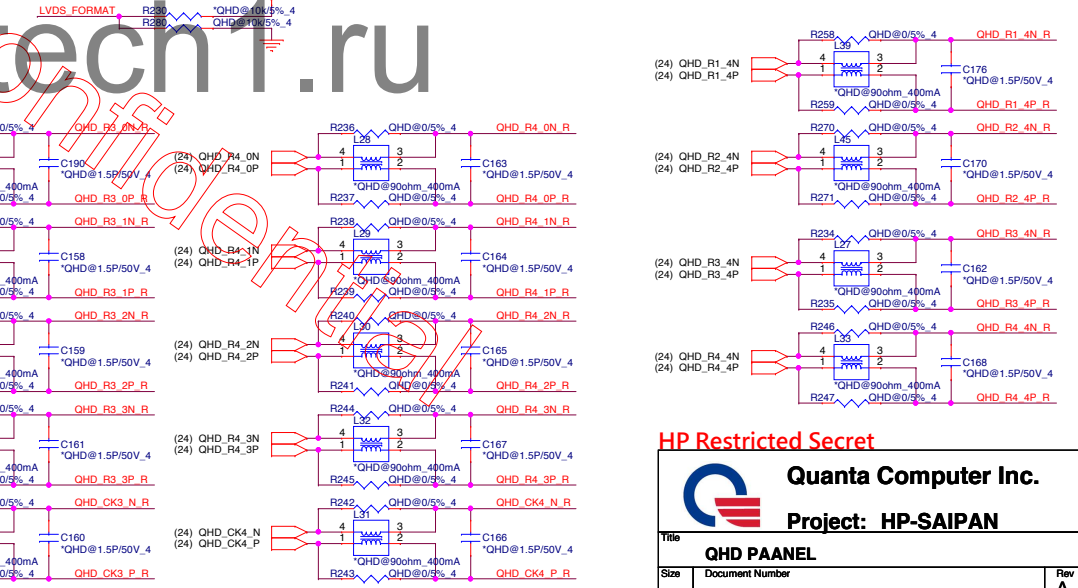
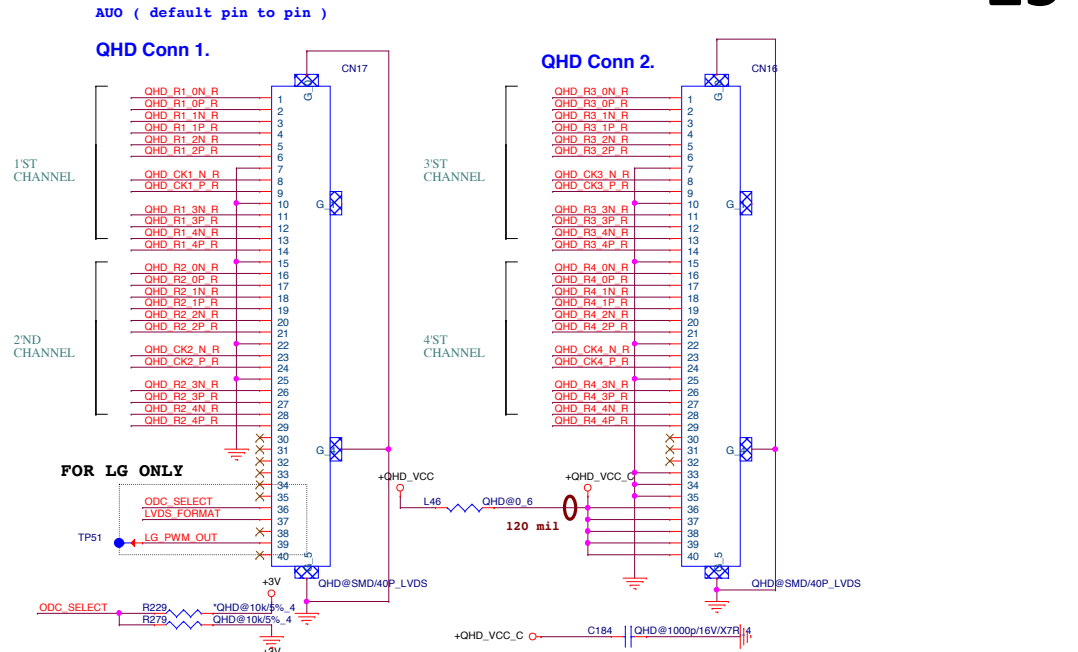
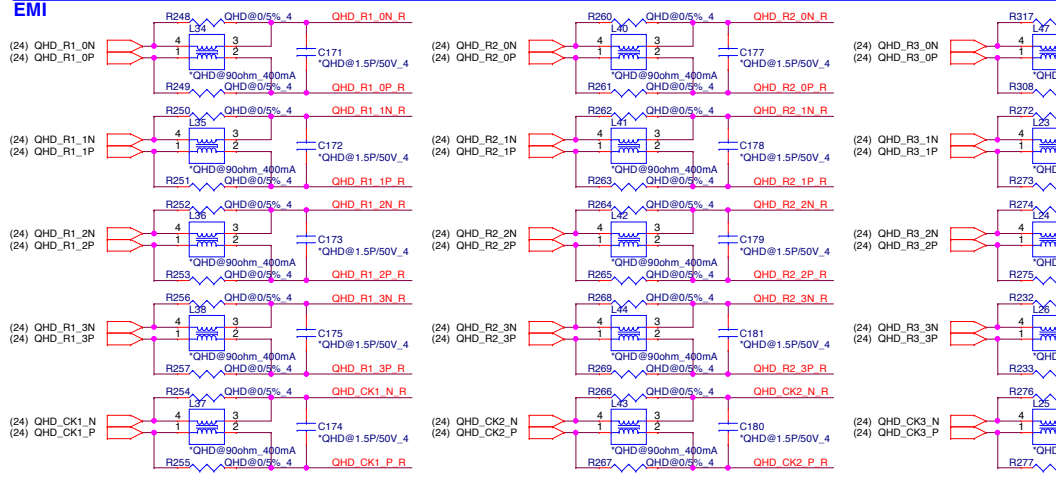
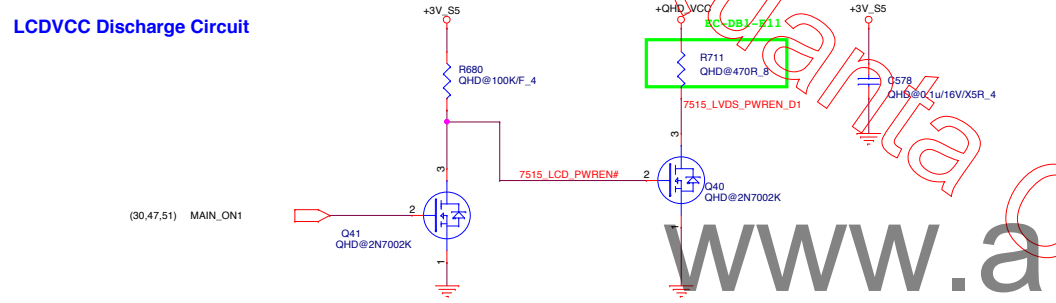






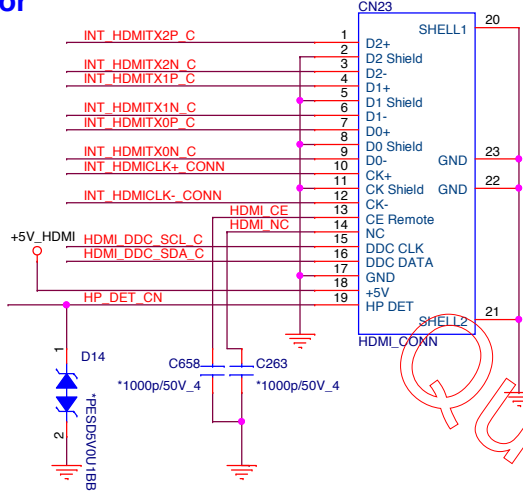
## LED PANEL

### PANEL VCC CONTROL

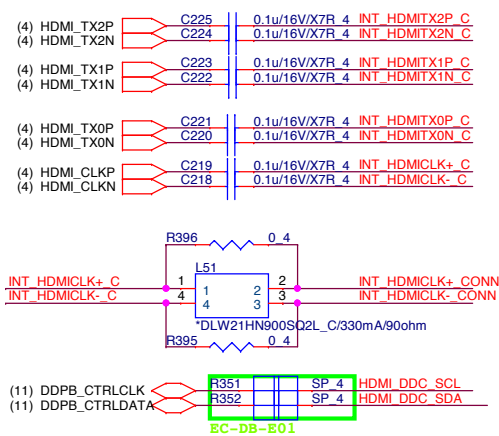




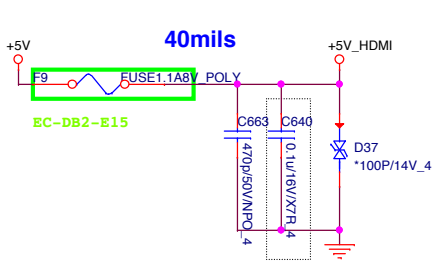
HDMI connector



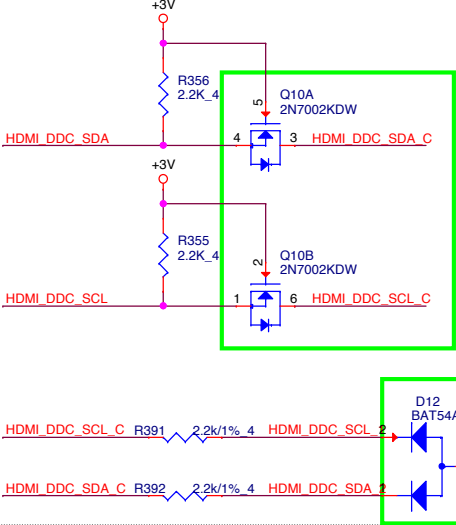
HDMI INTERFACE



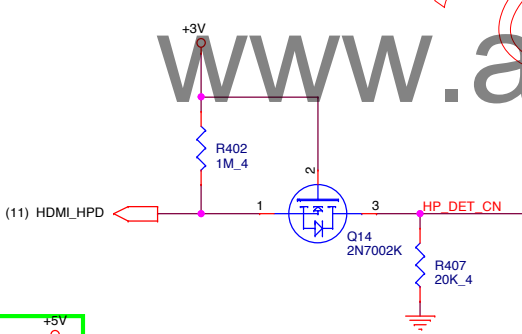
HDMI POWER SUPPLY



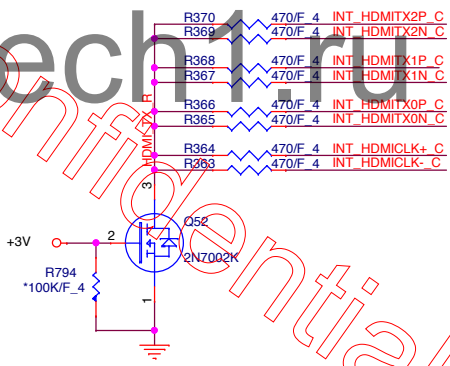
HDMI DDC



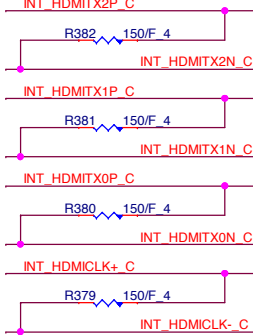
HDMI-detect



HDMI LEVEL SHIFT

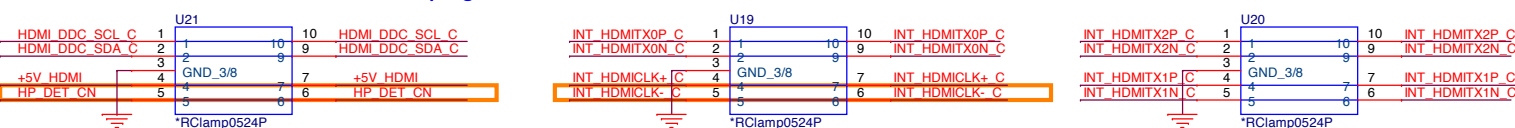


HDMI EMI (EMC)




ESD reserve for HDMI

Layout Notes:  
Place decoupling CAPs close to Connector



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**Quanta Computer Inc.**  
**Project: HP-SAIPAN**

Title: **HDMI**

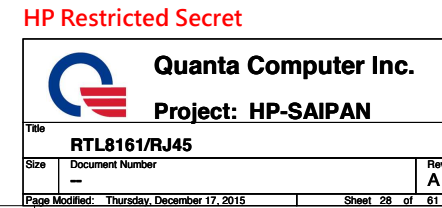
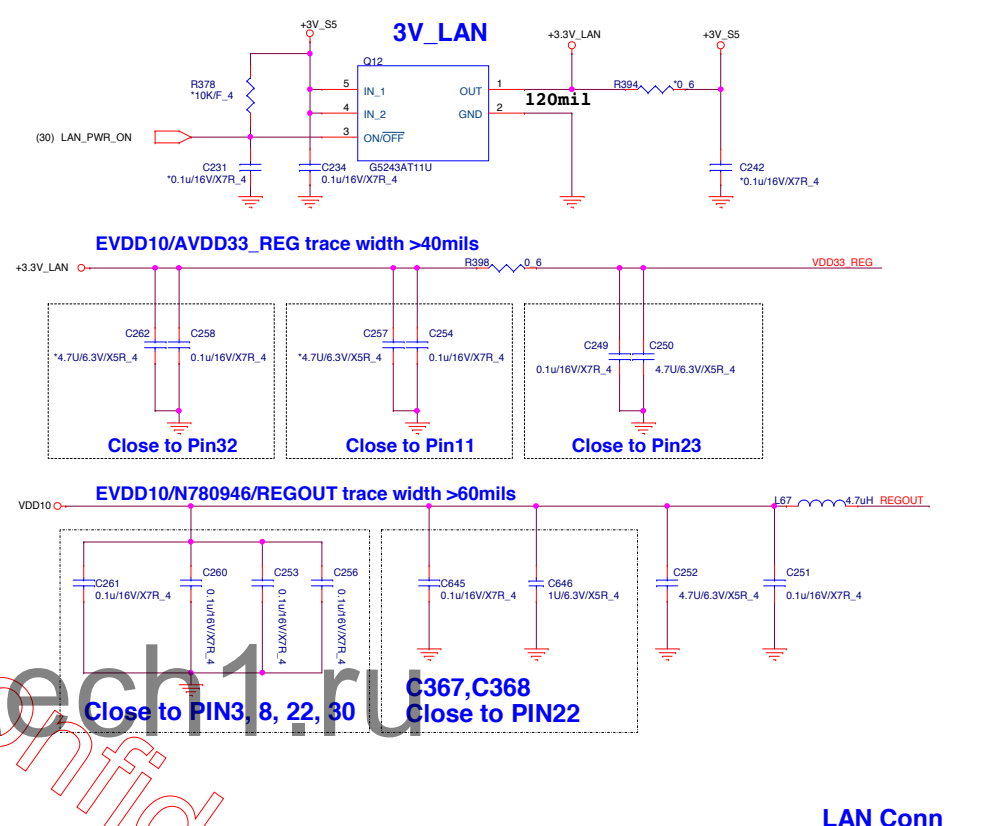
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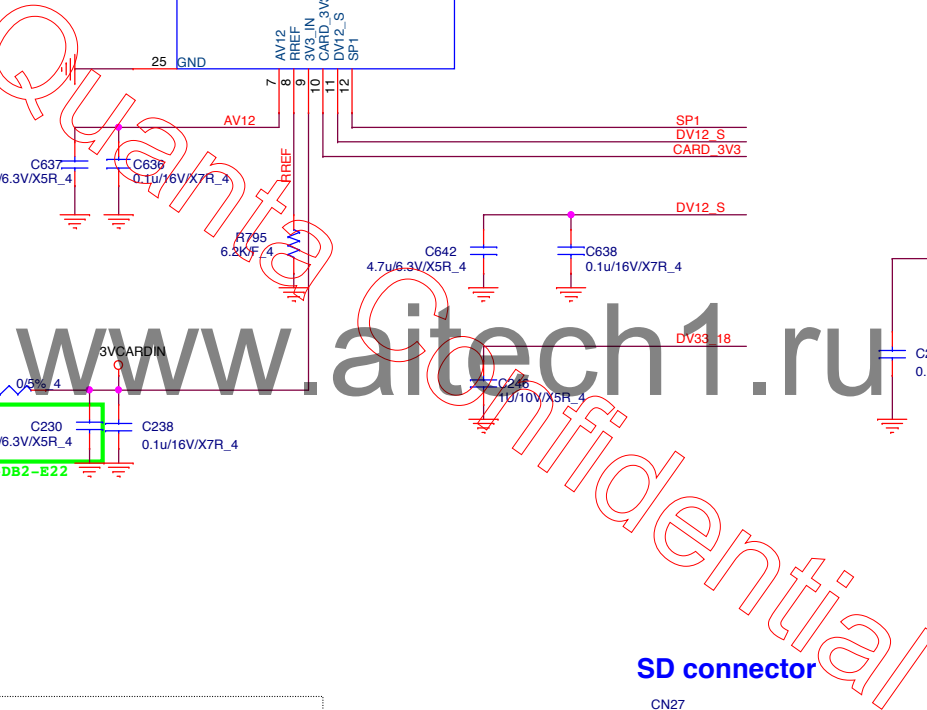






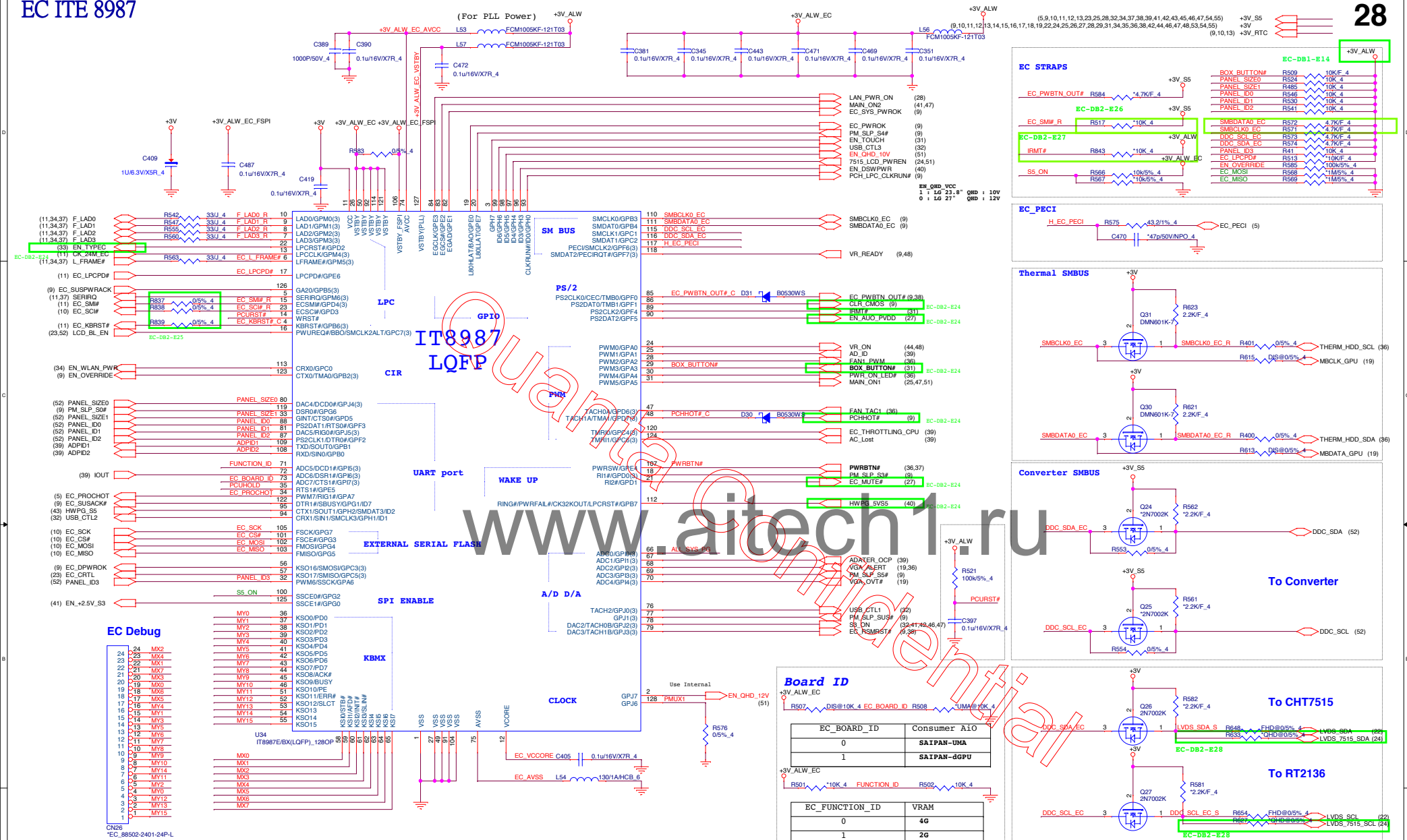






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## 3D CAM



## HD



Connector1:  
ACES 50376-00601-001

Pin	Definition
1	VCC_3.3V
2	D-
3	D+
4	MDATA
5	MCLK
6	GND

Connector2:  
ACES 50376-00601-001

Pin	Definition	MB
1	VCC_3.3V	16
2	D-	15
3	D+	14
4	IR_3.3V	13
5	IR_GND	11
6	DGND	10

**LEDs**



## ESD HD CAM

**Project: HP-SAIPAN**

eDP-LVDS RTD2136N

Size	Document Number
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Re  
Δ



# USB PORT

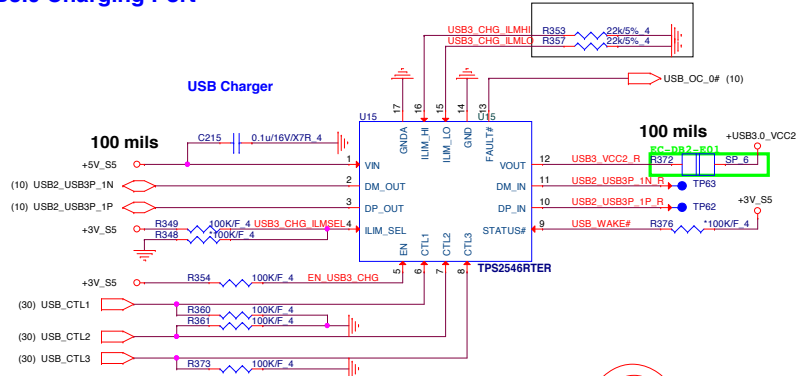
## USB3.0 Charging Port

(5,9,10,11,12,13,23,25,28,30,34,37,38,39,41,42,43,45,46,47,54,55) +3V\_S5  
(27,31,33,36,39,40,41,43,44,45,46,47,54) +5V\_S5



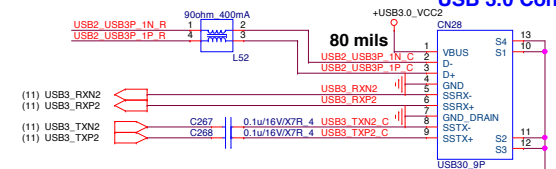
32

### USB 3.0 Conn.

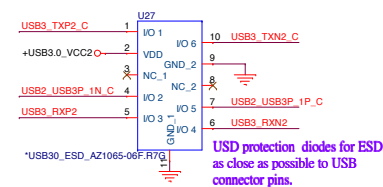


SDP : Standard Downstream Port  
CDP : Charging downstream port  
DCP : Dedicated Charging Port  
Enable/Disable : setting by BIOS

POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS	0	0	1	1

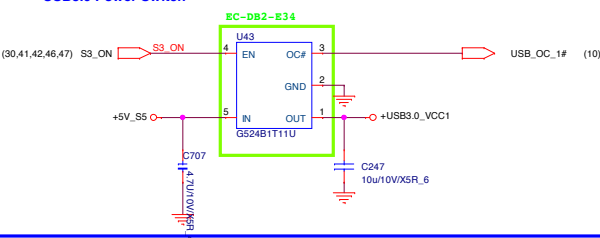


### ESD

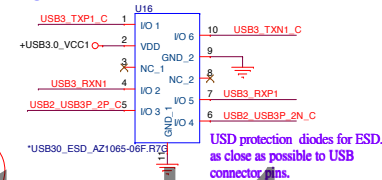


## USB3.0 PORT

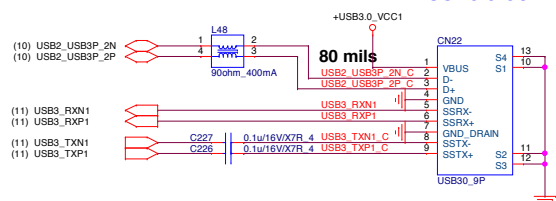
### USB3.0 Power Switch



### ESD

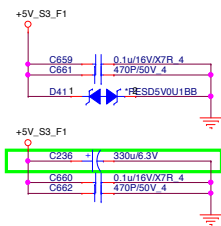
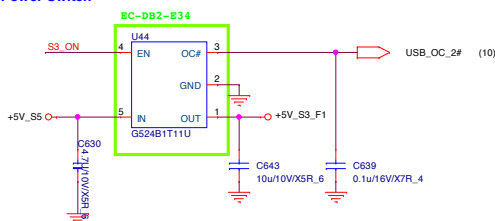


### USB3.0 Conn



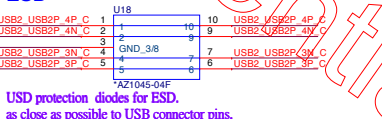
## USB2.0 X 2

### USB3.0 Power Switch

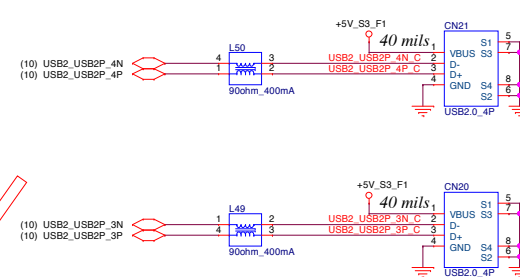


Layout:  
1. All caps Near to Connector  
2. Place D40 near CN21 and CN22

### ESD



### USB2.0 Conn



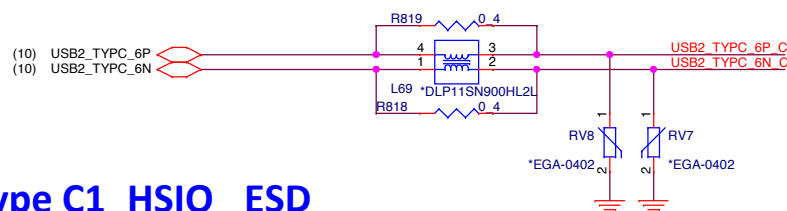
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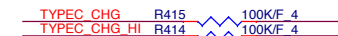
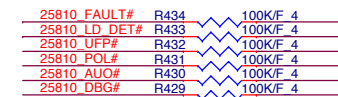
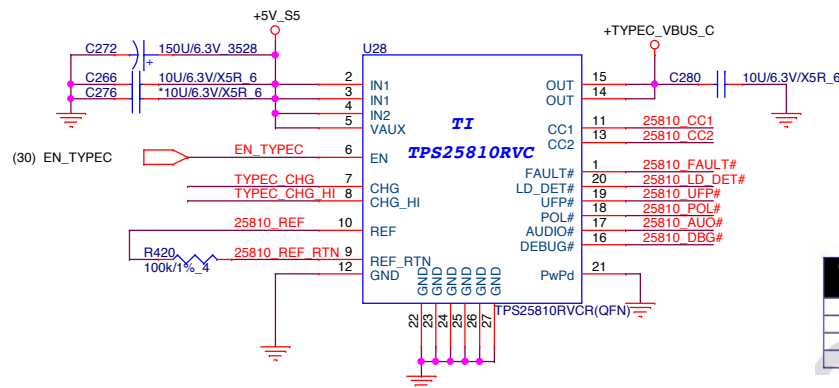
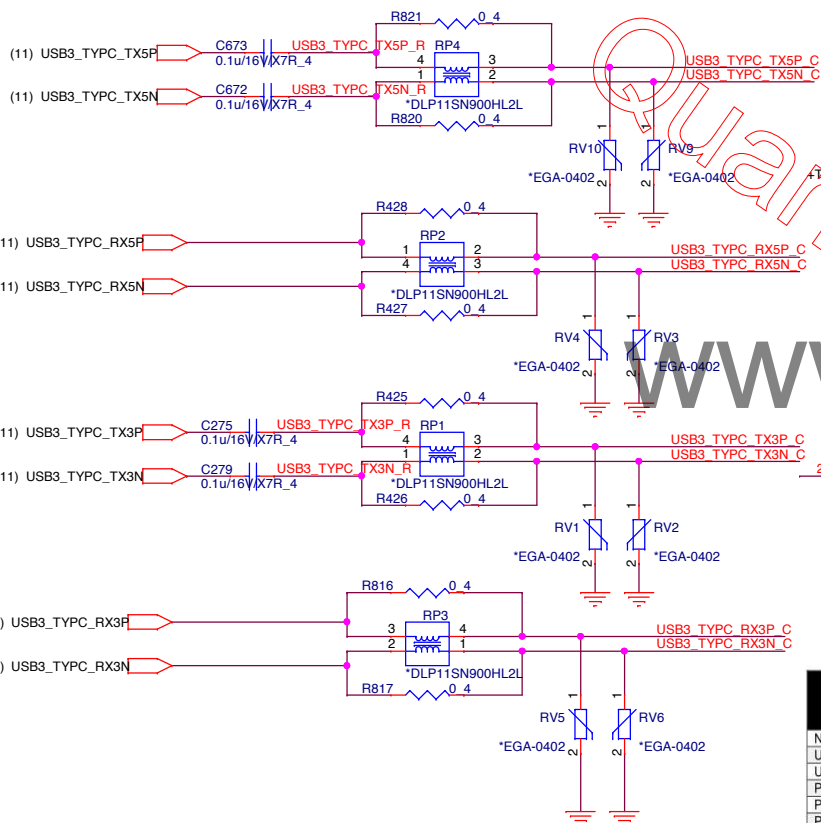
Title	USB2.0/USB3.0 Conn	
Size	Document Number	Rev A
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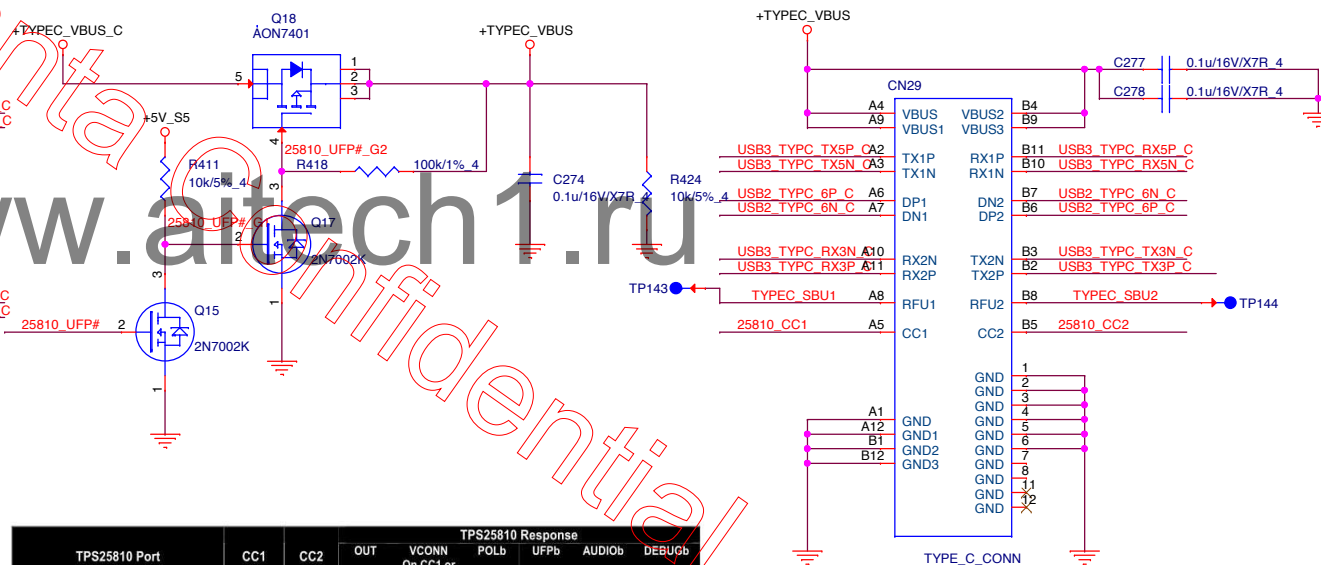
## USB2.0 ESD



## Type C1\_HSIO\_ESD



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

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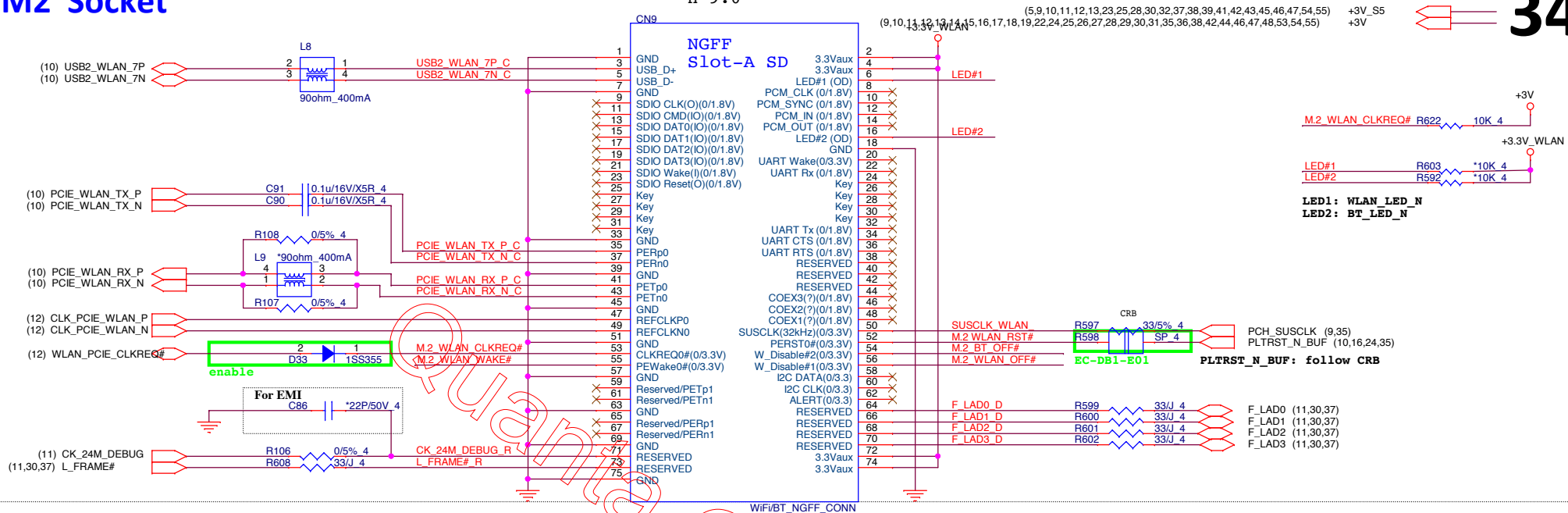
Title		
USB TYPE-C		
Size	Document Number	Rev
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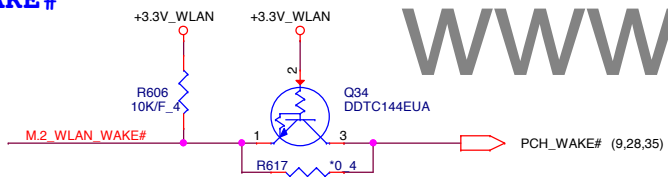
## NGFF M2 Socket

H=9.0

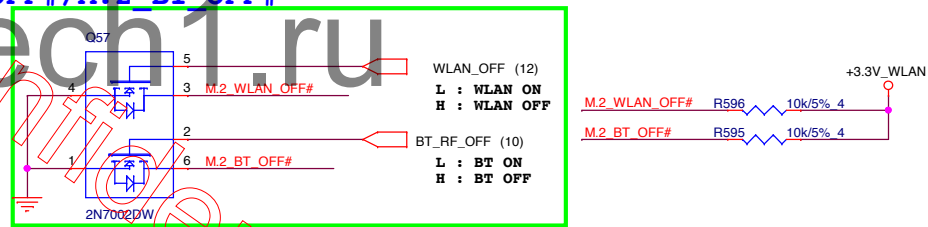
34



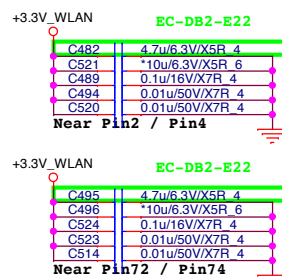
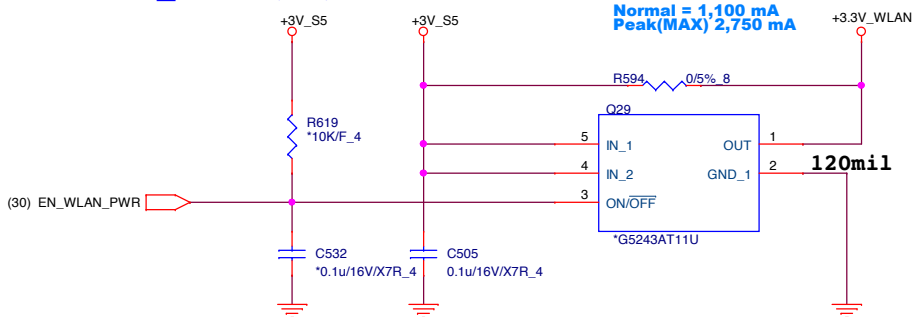
## M.2 WLAN WAKE#



**M.2 WLAN OFF#/M.2 BT OFF#**



## NGFF M2\_power(S5)



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Title	NGFF M.2 WLAN
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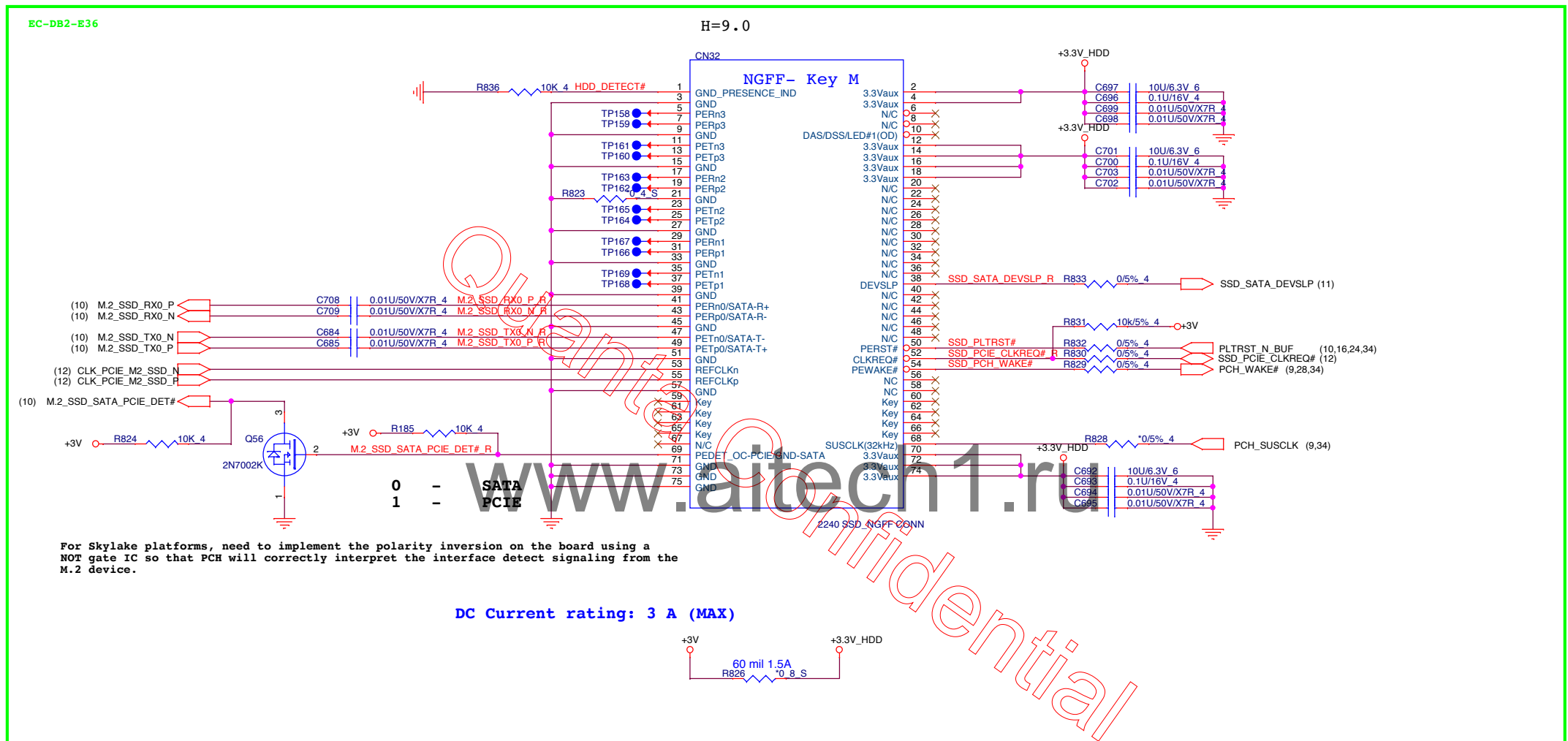
Size	Document Number
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Rev <b>B</b>
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Title	NGFF M.2 WLAN
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Size	Document Number
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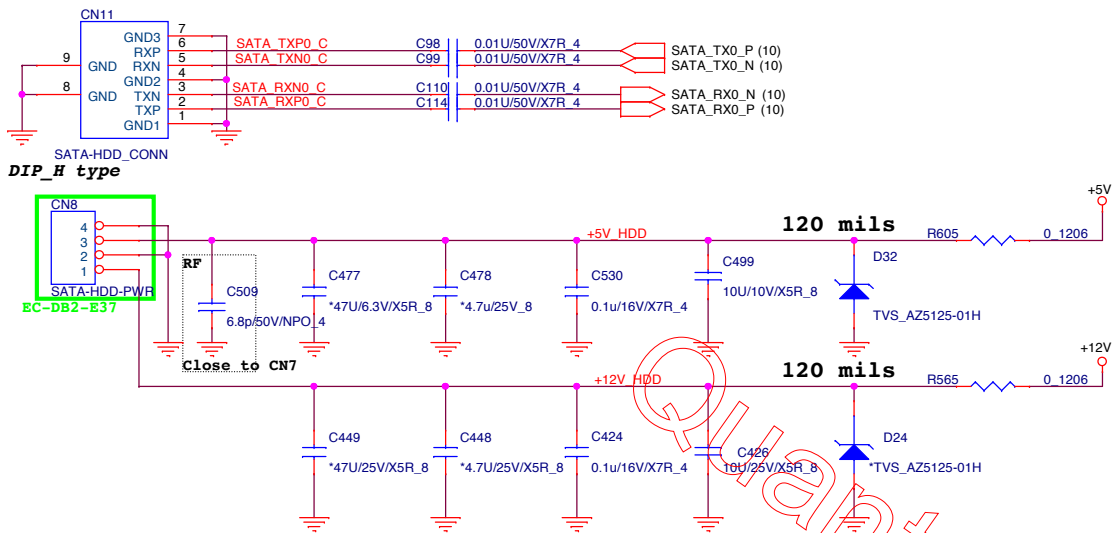
Rev  
B

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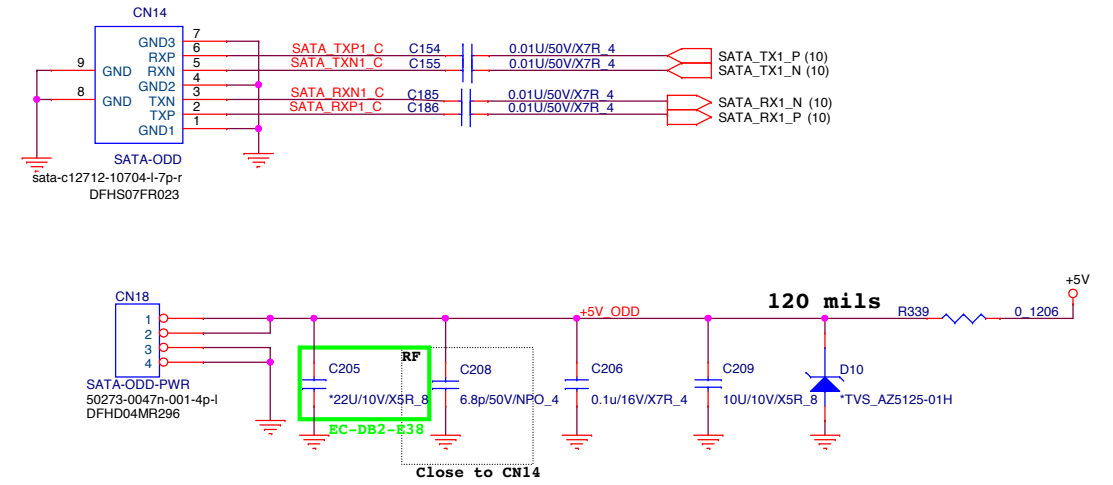
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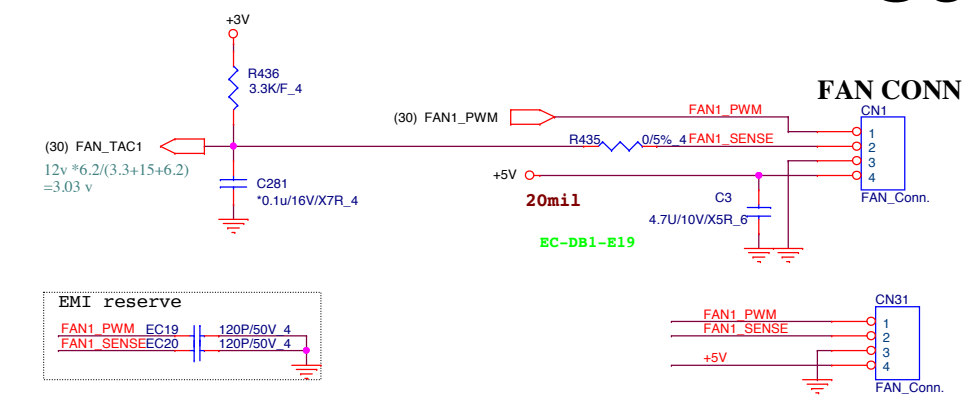
SATA HDD  
HDD SATA Conn.



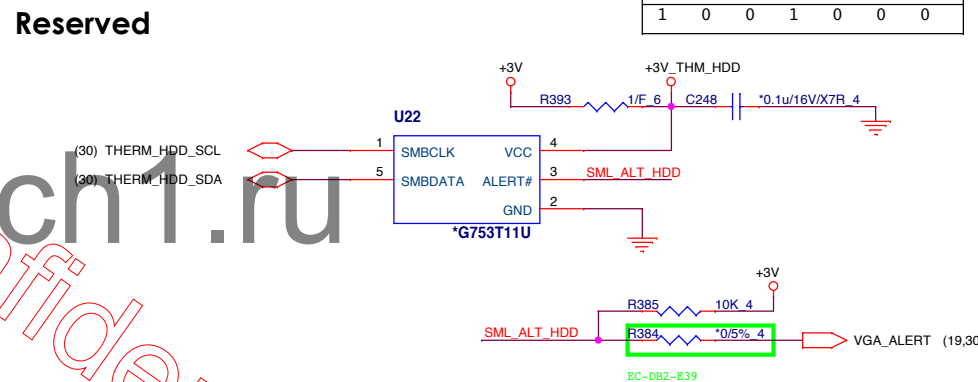
SATA ODD  
ODD SATA Conn.



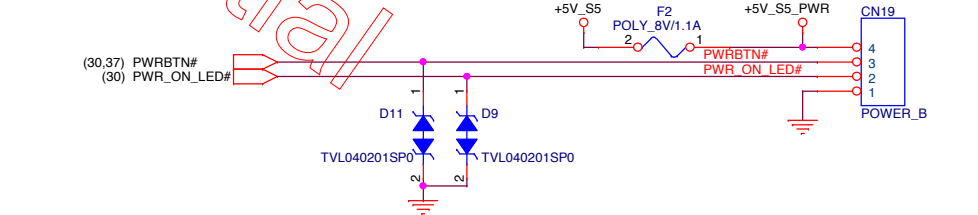
SYSTEM FAN



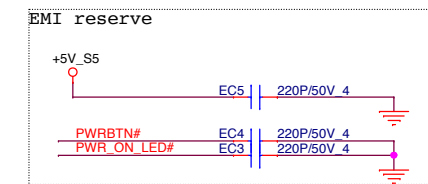
Ambient SENSOR




Power Button.



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**Project: HP-SAIPAN**

Title		FAN/HDD/ODD/HDD CONN.	
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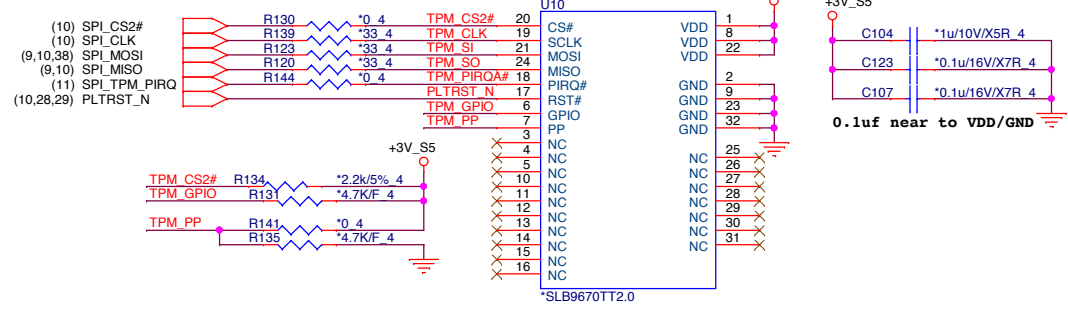
# TPM2.0

(5,9,10,11,12,13,23,25,28,30,32,34,38,39,41,42,43,45,46,47,54,55)  
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55)  
(23,26,27,31,36,39,46,47,48,49,50,53,55)  
(5,7,9,38,46,47,48)

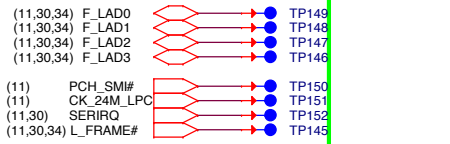


37

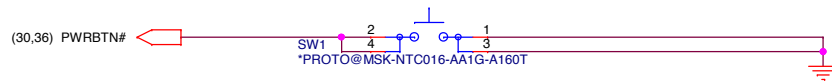
## SPI TPM2.0



## LPC HEADER



SW1 For Debug.MP will remove it.



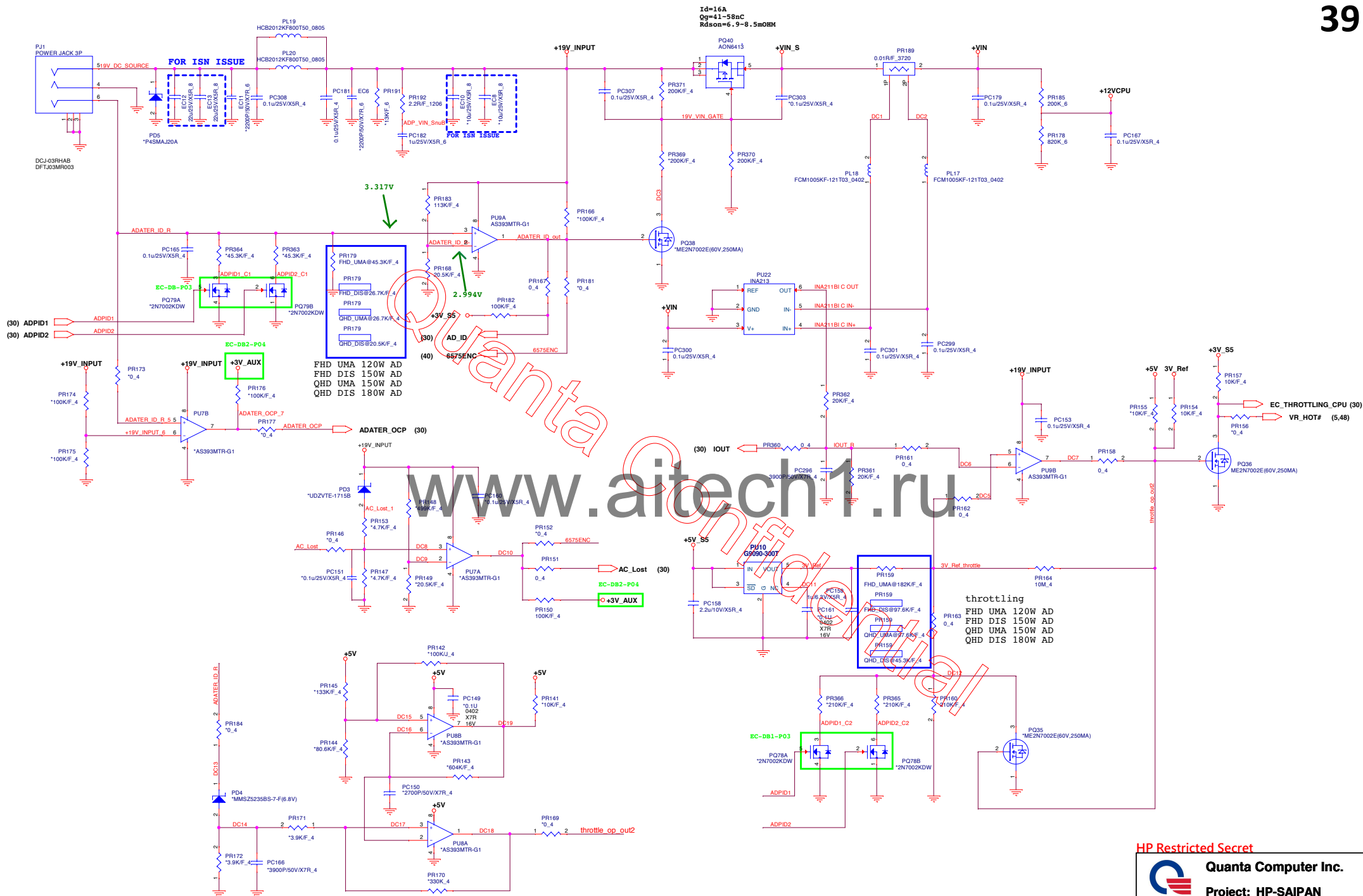
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		<b>Quanta Computer Inc.</b> <b>Project: HP-SAIPAN</b>
<b>Title</b> Debug /LPC Header/TPM		
<b>Size</b> ---	<b>Document Number</b> ---	<b>Rev</b> A
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HP Restricted Secret

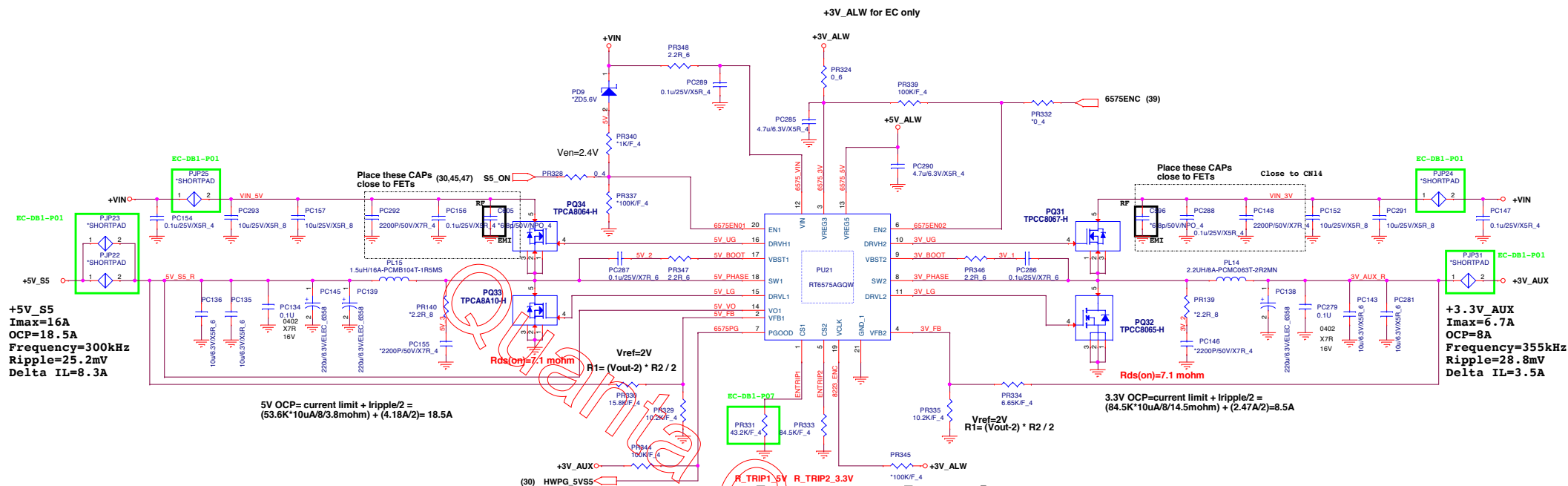


**Quanta Computer Inc.**

**Project: HP-SAIPAN**

Title			Project: HF-SAIPAN		
DC-IN					
Size	Document Number				Rev
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L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8065-H	DFN3x3	13A	14.5m
TPCA8A10-H	DFN5x6	40A	3.8m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

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**Quanta Computer Inc.**  
**Project: HP-Saipan**

Title  
**3V\_AUX/5V\_S5(RT6575AGQW)**

Size Document Number Rev  
 --- A

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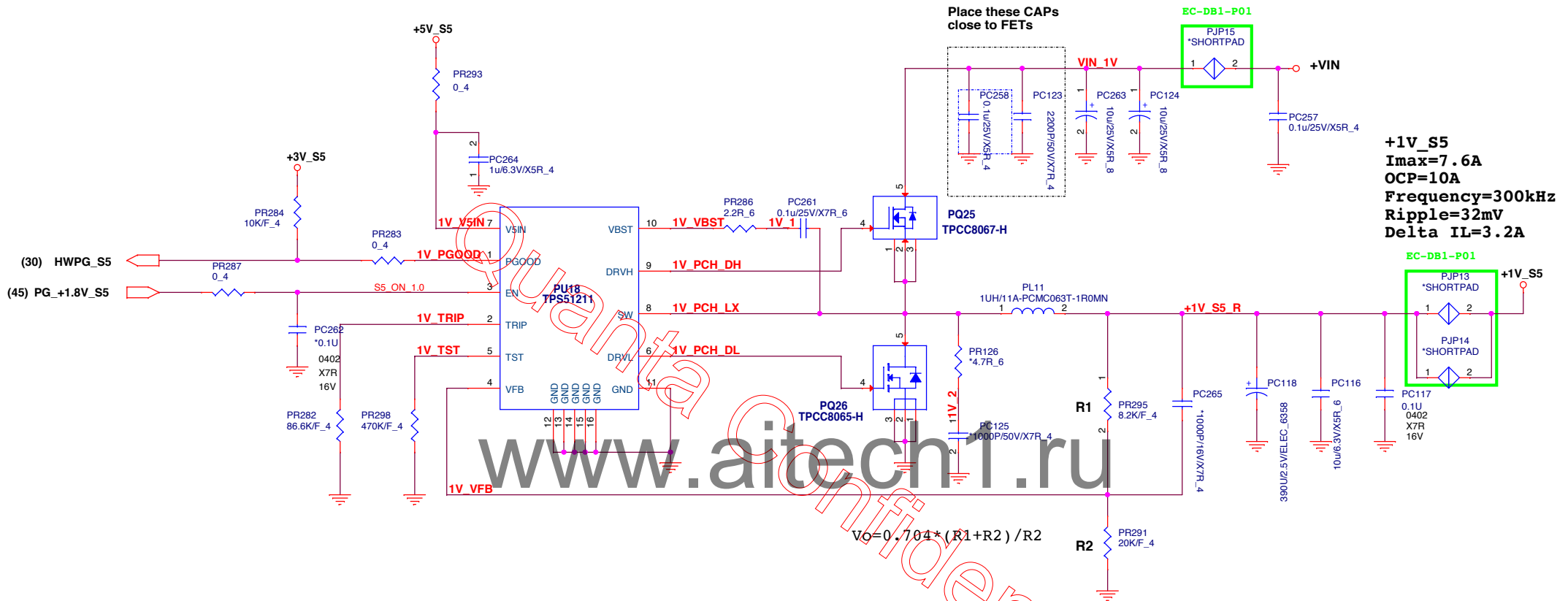




1	0	1	0.95V
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Project: HP-SAIPAN

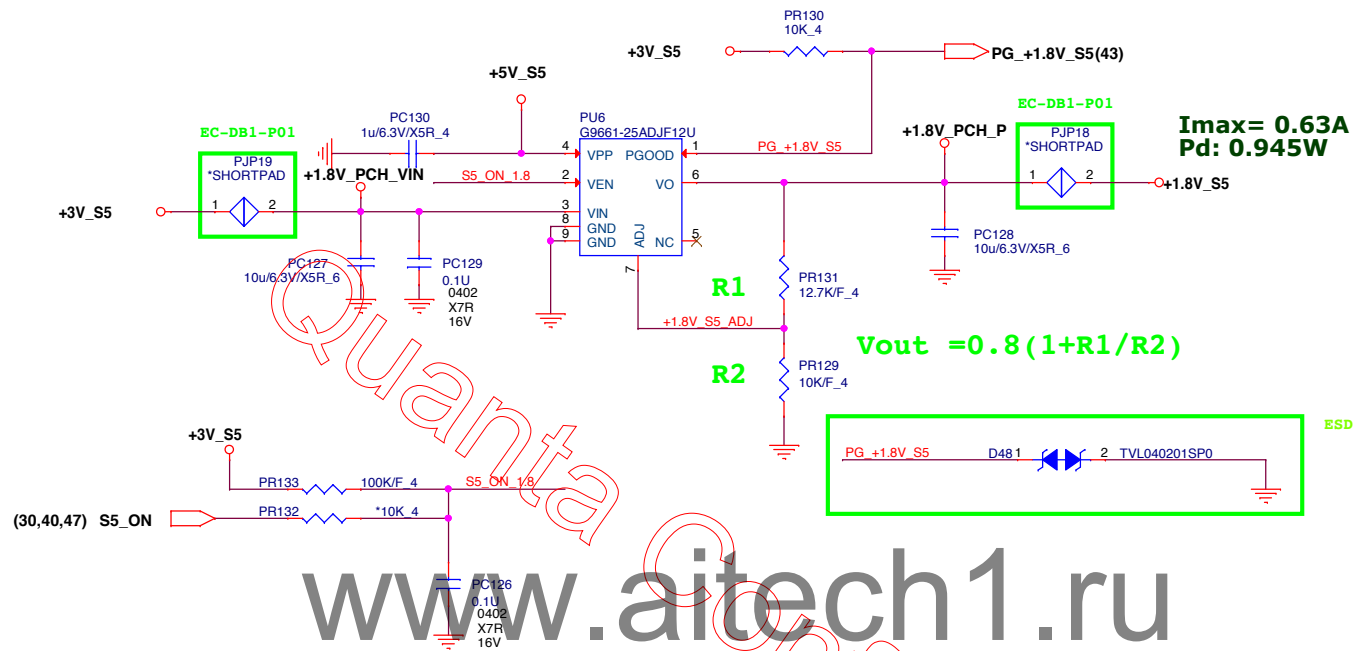
Title <b>+1V_S5(TPS51211)</b>		
Size	Document Number	Rev <b>A</b>
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Project: HP-Saipan

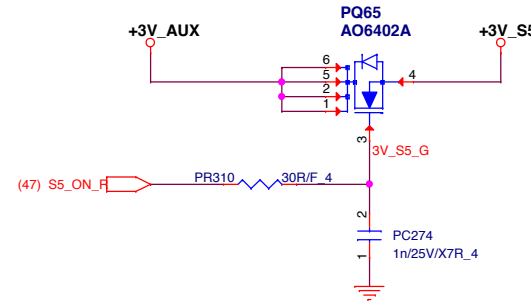
Title <b>+1.8V_S5 (G9661)</b>		
Size	Document Number	Rev
---	---	<b>A</b>
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## S5 ON Load SW

AO6402A  
Rdson=24m@10V Vgs  
Imax=5.5A  
Pd: 0.726W

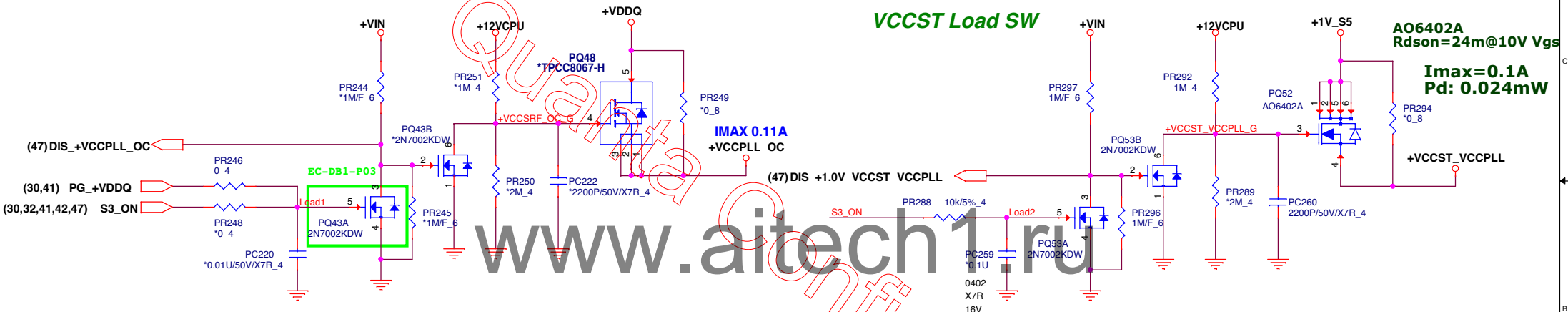
46



## VCCST Load SW

## VCCST Load SW

AO6402A  
Rdson=24m@10V Vgs  
Imax=0.1A  
Pd: 0.024mW



## MAIN ON\_1 Load SW

AO6402A  
Rdson=24m@10V Vgs

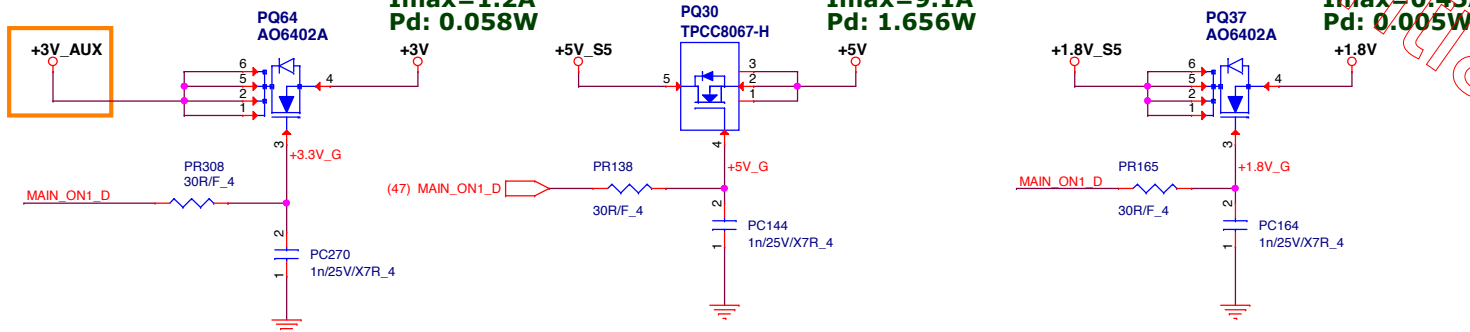
Imax=1.2A  
Pd: 0.058W

TPCC8067-H  
Rdson=20m@10V Vgs

Imax=9.1A  
Pd: 1.656W

AO6402A  
Rdson=24m@10V Vgs

Imax=0.45A  
Pd: 0.005W



## Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8064-H	SO-8	20A	7.9m	+/- 20V

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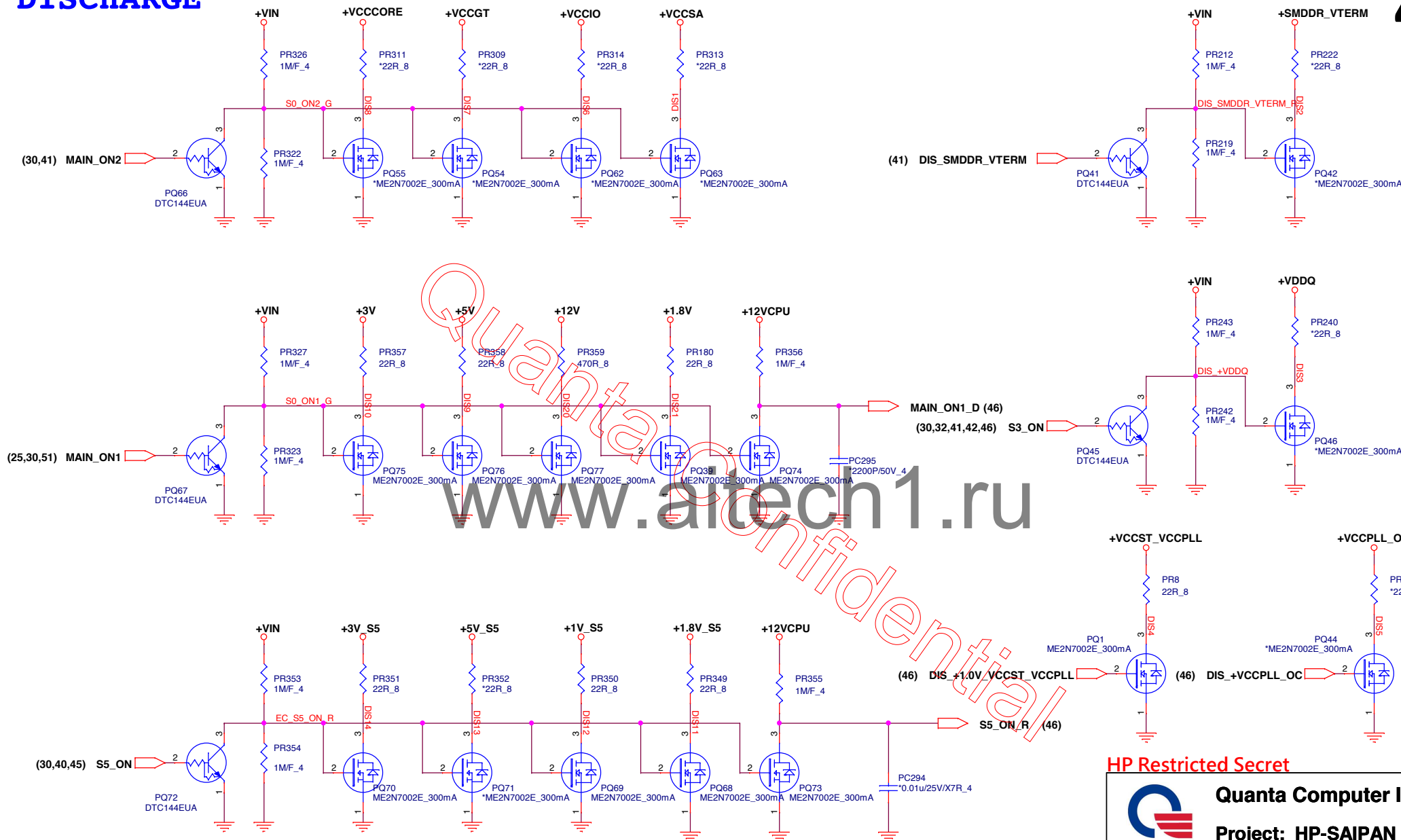
Project: HP-SAIPAN

Title	Load Switch		
Size	Document Number	Rev	
---	---	A	
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# DISCHARGE

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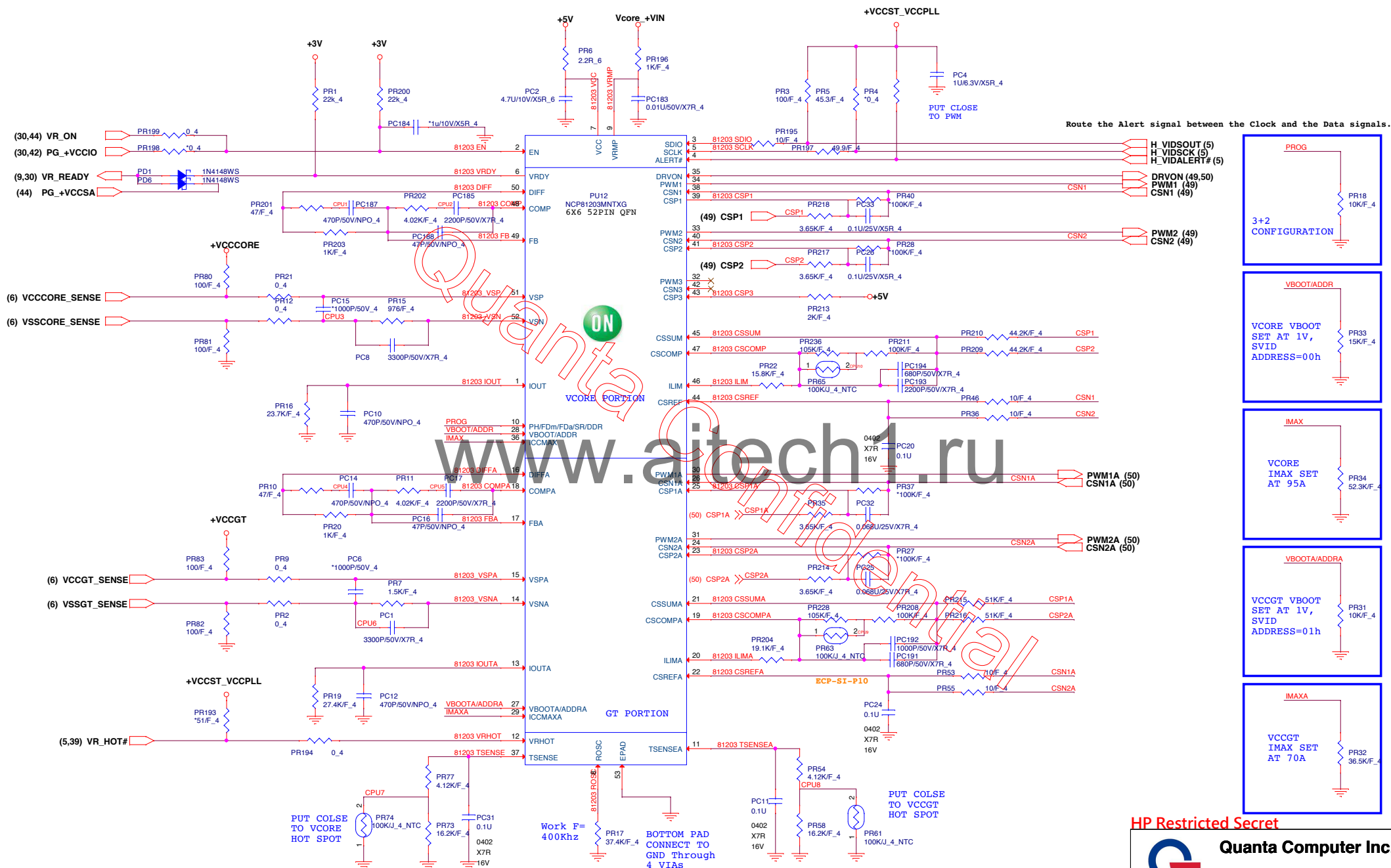
Project: HP-SAIPAN

Title	Discharge	
Size	Document Number	Rev
---	---	A
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# Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE

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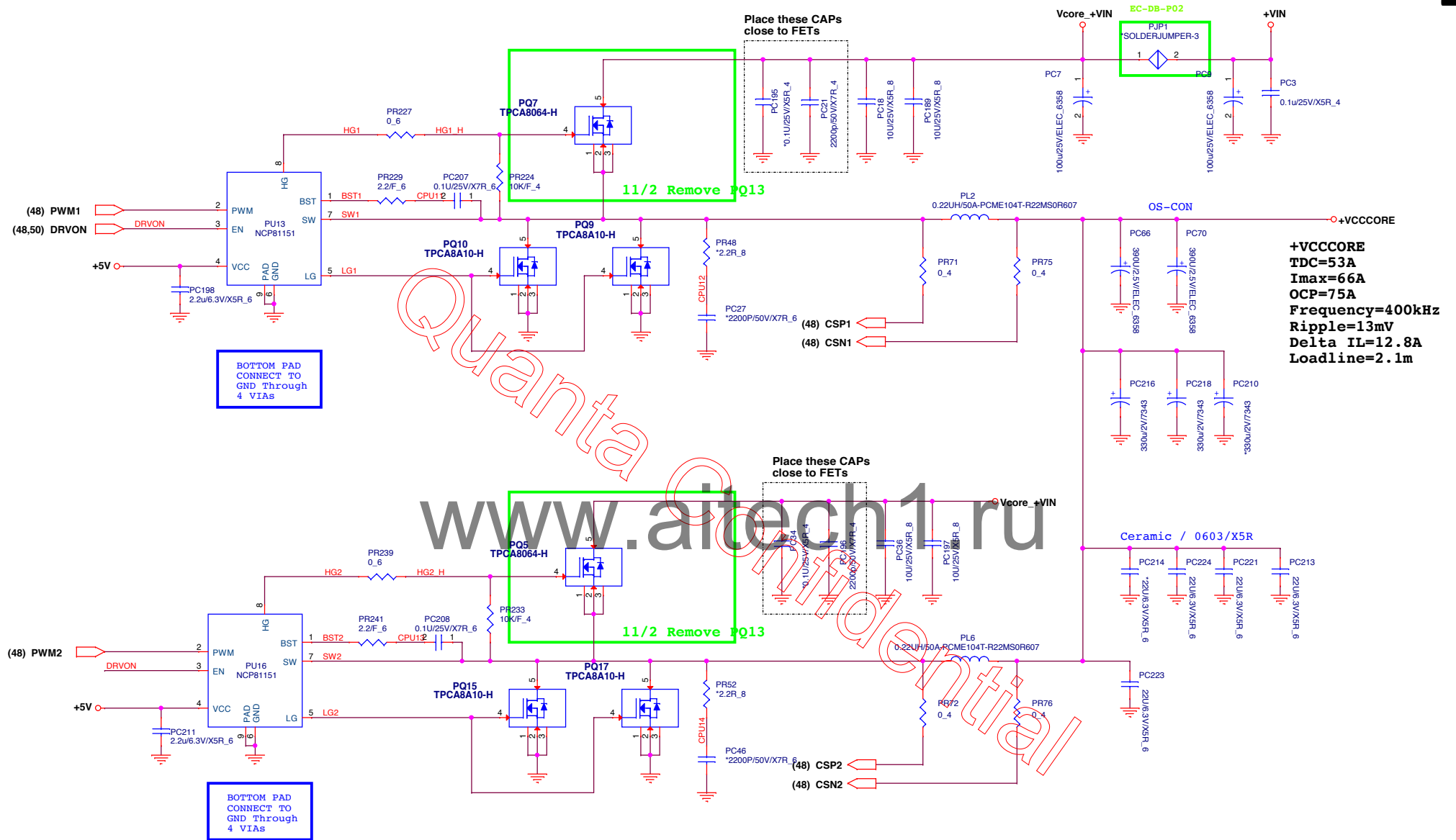


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Project: HP-Saipan

Title			Rev
VCC_CORE & VCC_GT			
Size	Document Number		
--	--	A	
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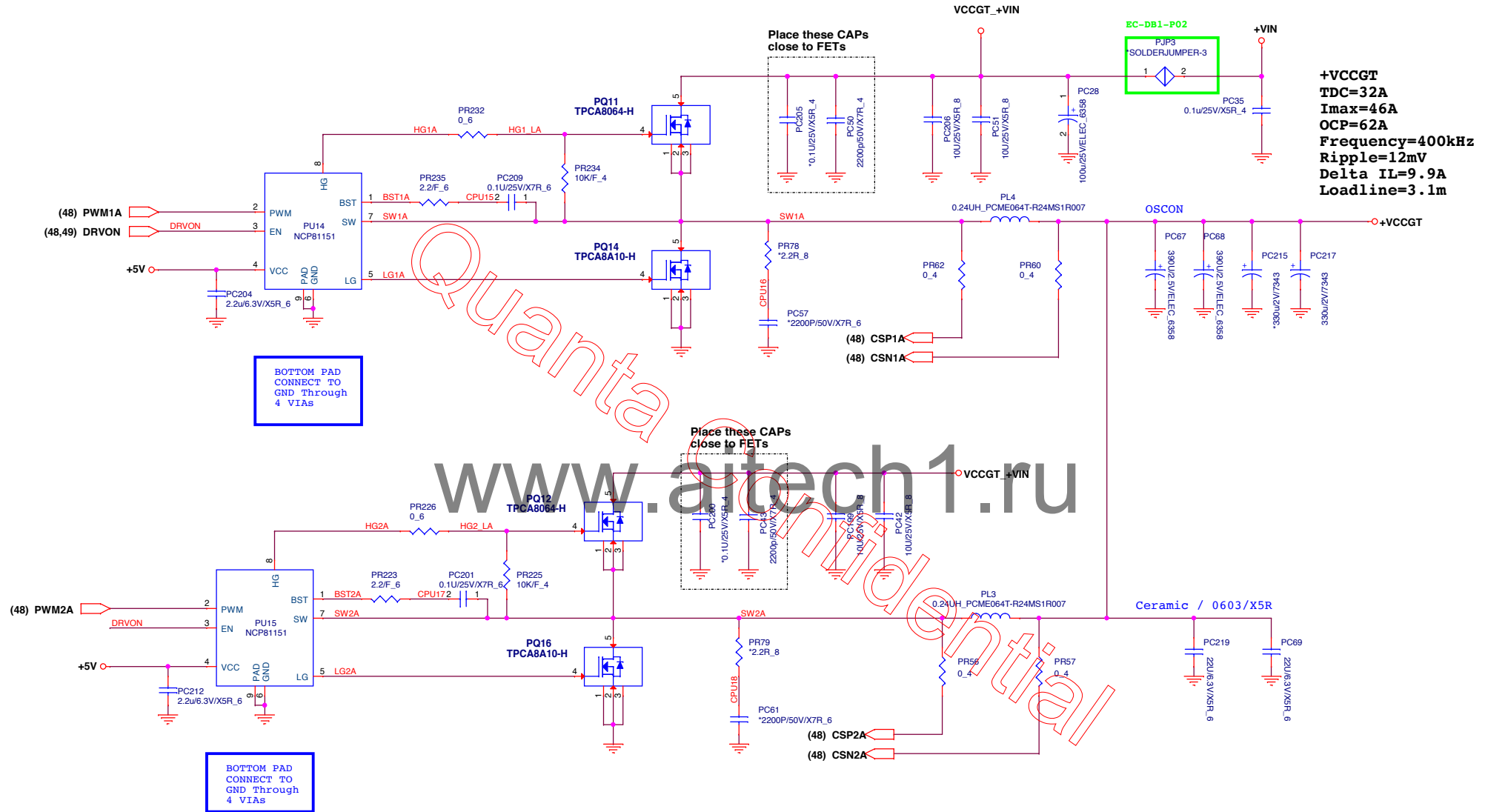


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Project: HP-Saipan

Title <b>VCORE OUT STAGE</b>		
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Project: HP-Saipan

Title		
VCCGT OUTPUT STAGE		
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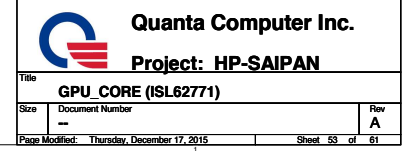






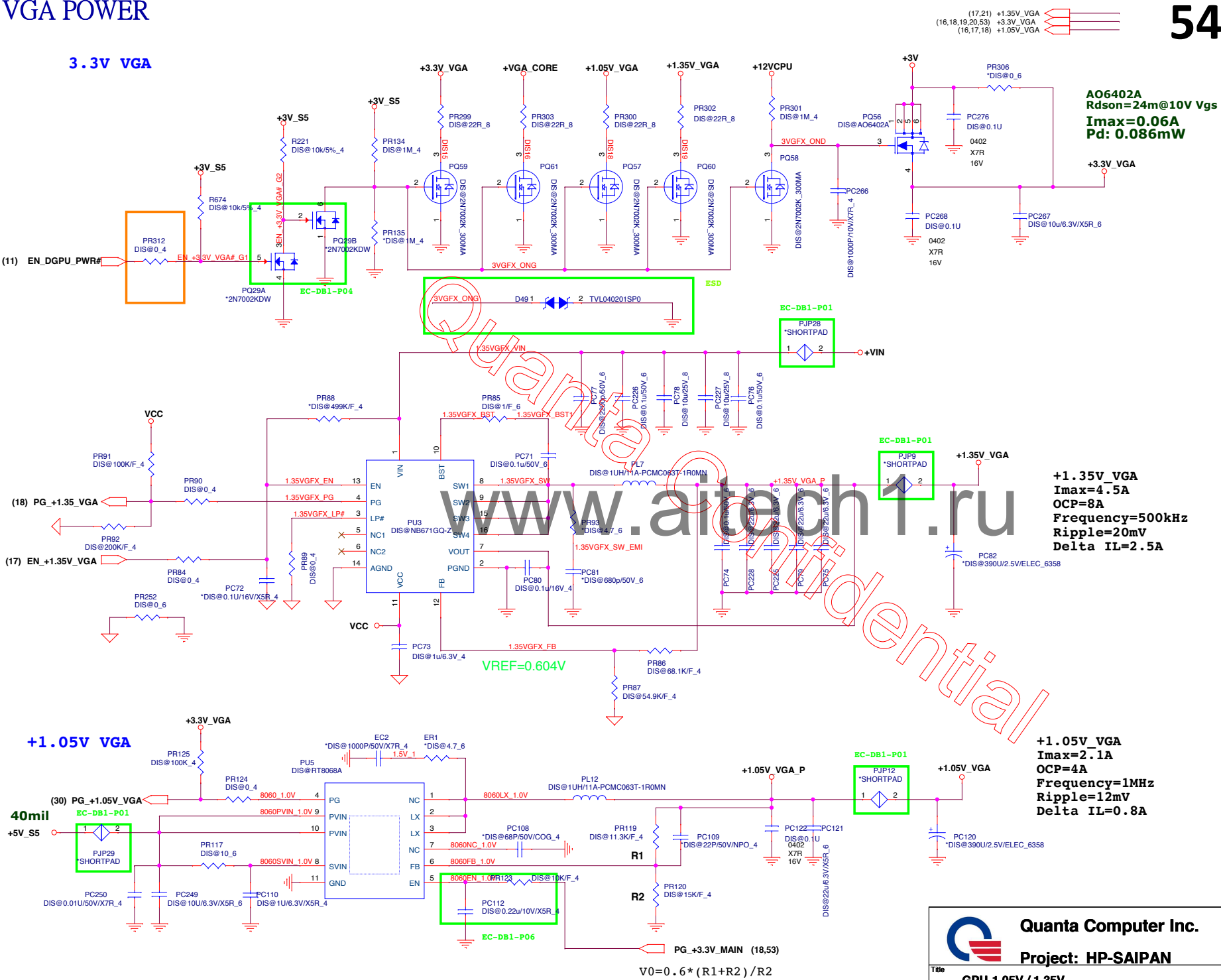








3.3V VGA



A06402A  
Rdson=24m@10V Vgs  
Imax=0.06A  
Pd: 0.086mW

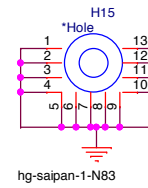
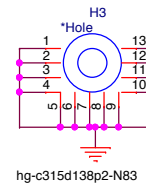
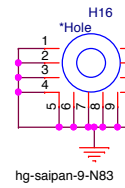
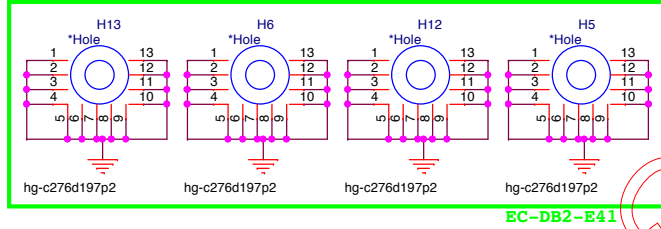
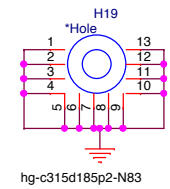
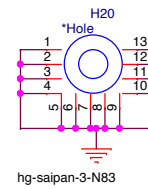
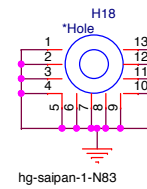
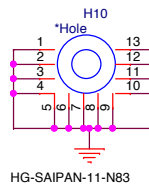
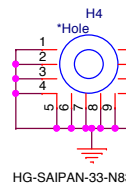
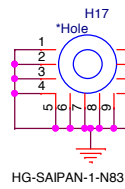
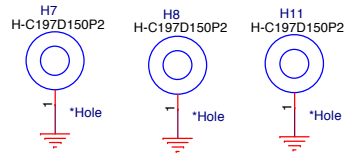
+1.35V\_VGA  
Imax=4.5A  
OCP=8A  
Frequency=500kHz  
Ripple=20mV  
Delta IL=2.5A

+1.05V\_VGA  
Imax=2.1A  
OCP=4A  
Frequency=1MHz  
Ripple=12mV  
Delta IL=0.8A

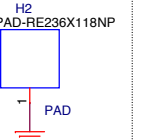
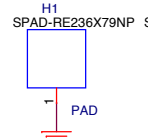
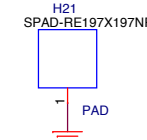
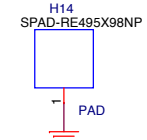
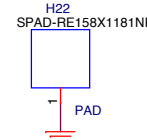
$$V0 = 0.6 * (R1 + R2) / R2$$



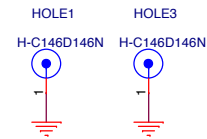
## CPU HOLE



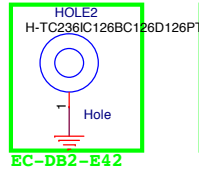
## EMI PAD



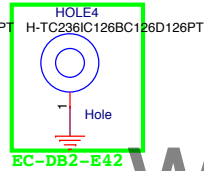
## VGA HOLE



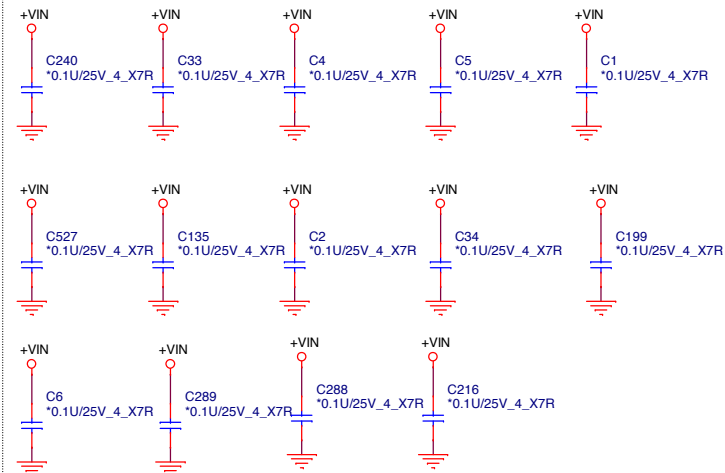
## WLAN HOLE



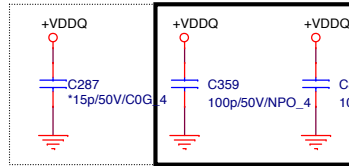
## SSD HOLE



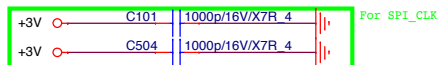
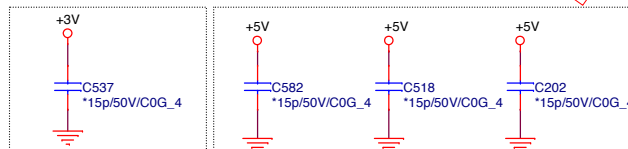
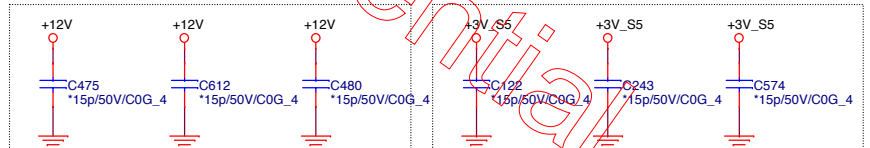
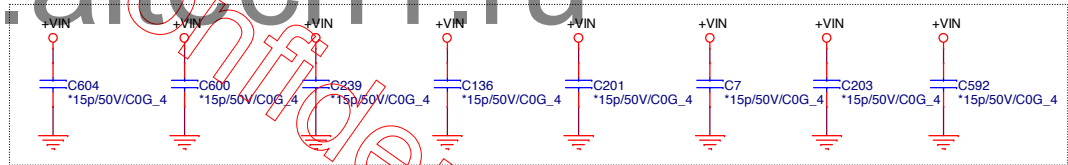
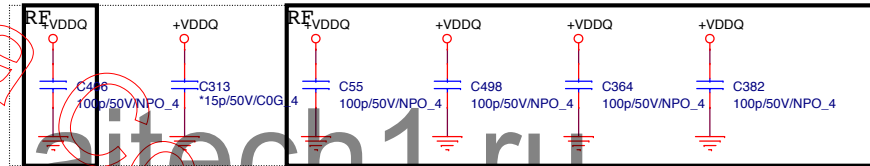
## Place around +VIN trace



## RF



## RF



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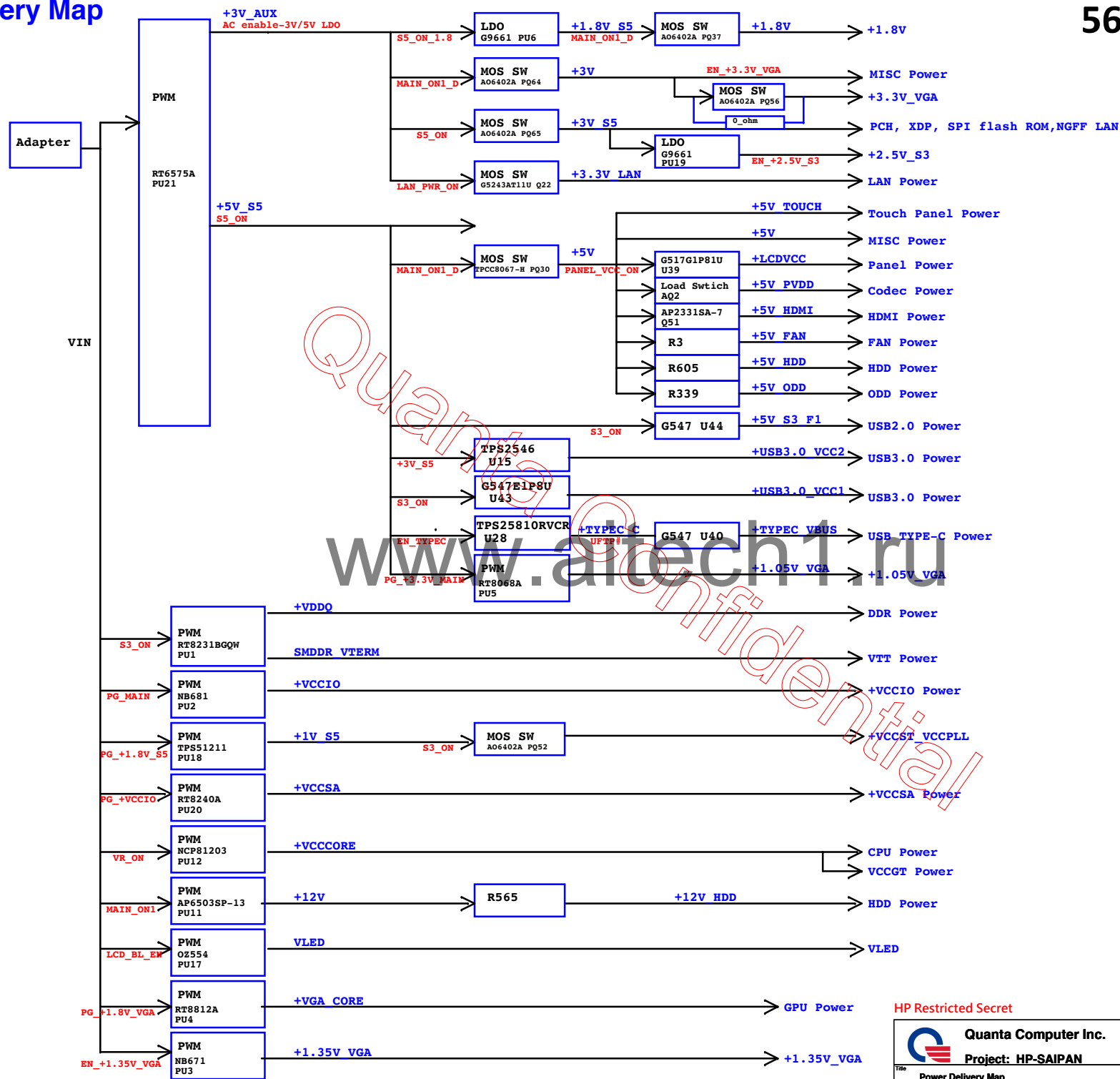


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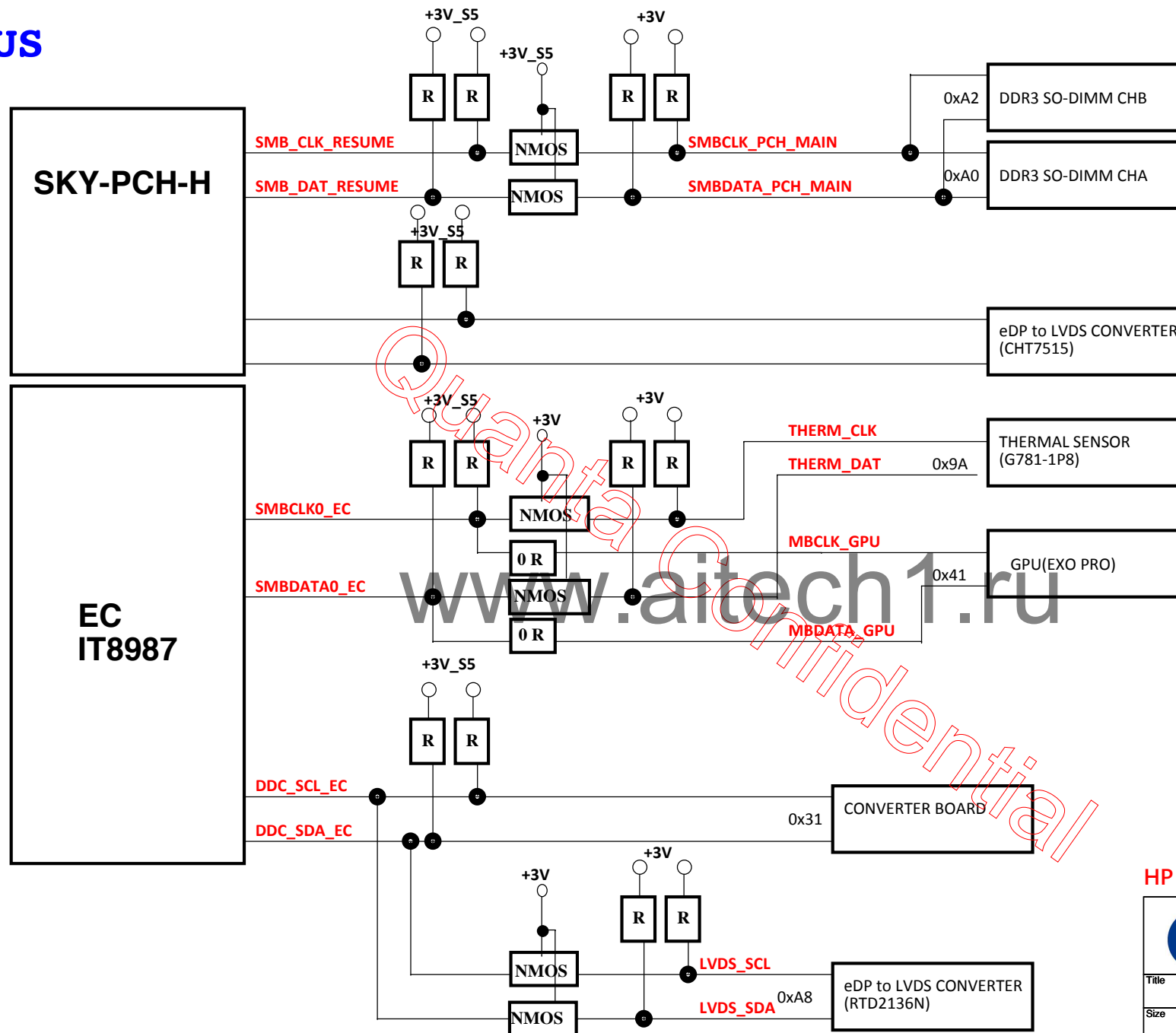
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Title HOLE/VIN CAP/RF CAP		
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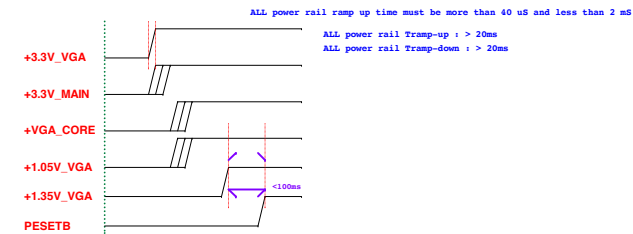
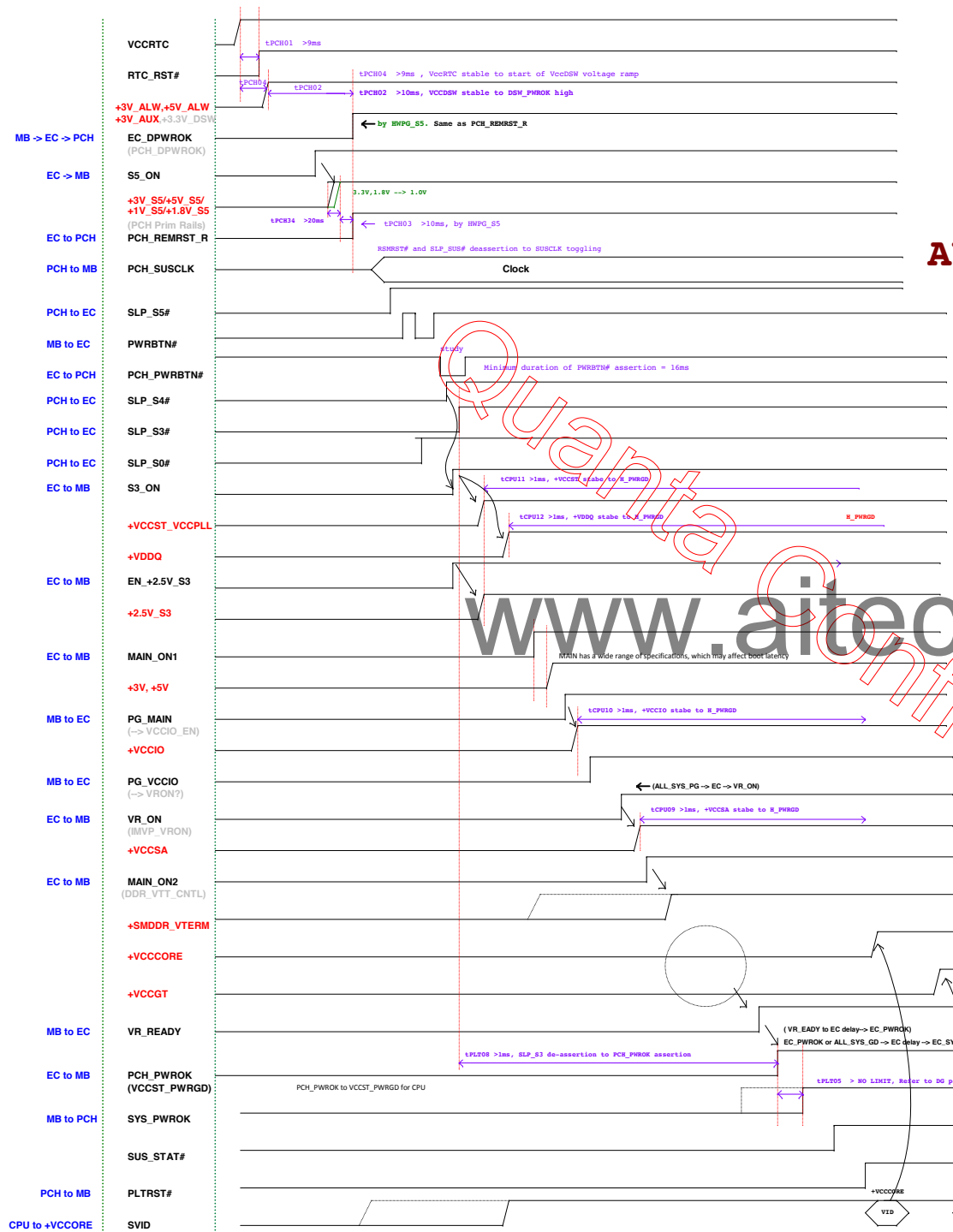
Project: HP-Saipan

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Size	Document Number	Rev
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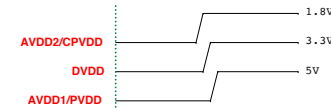


## Nvidia dGPU POWER SEQUENCE 58

## Nvidia dGPU POWER SEQUENCE 58



## AUDIO POWER SEQUENCE

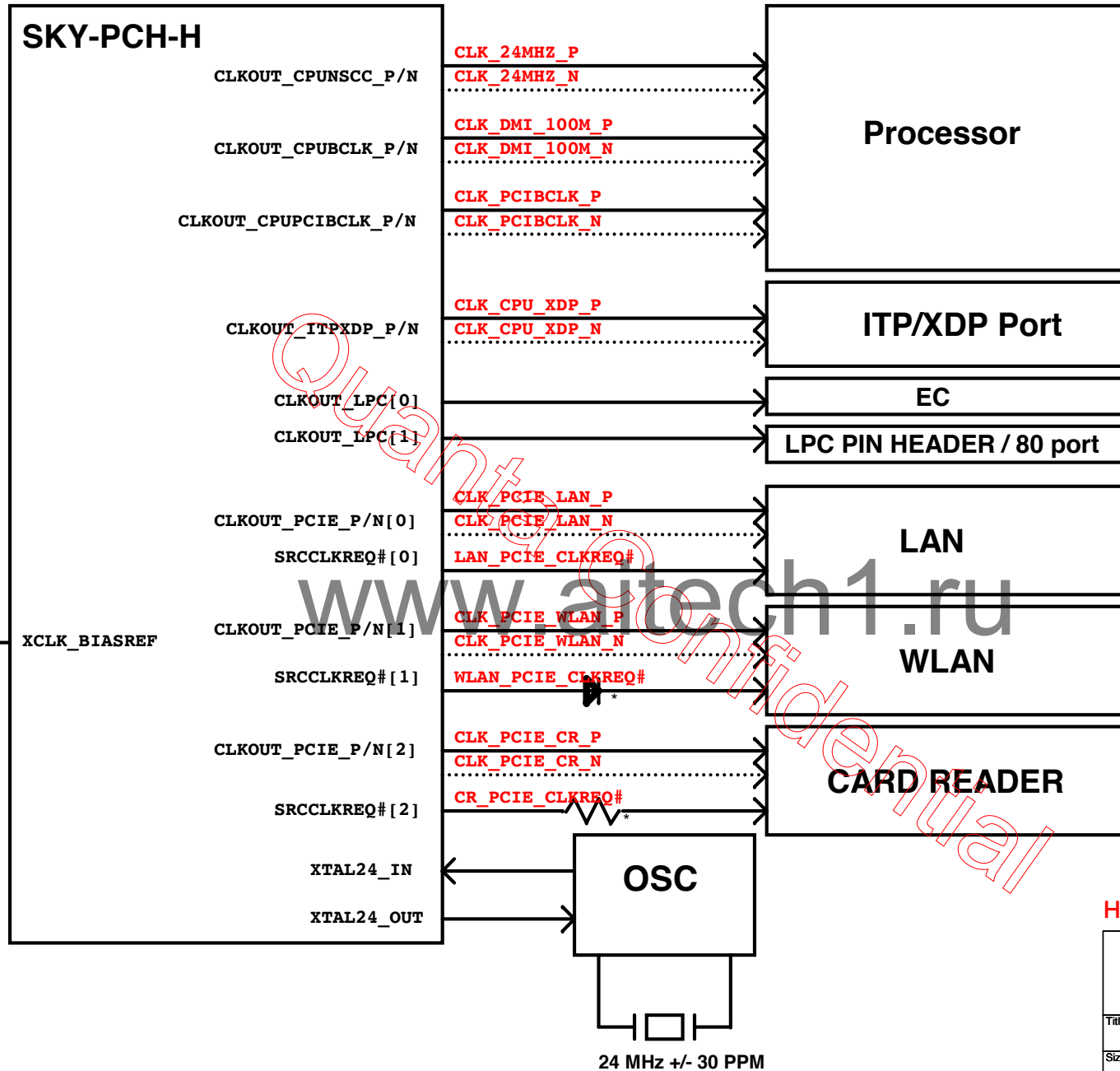


[www.aitech1.ru](http://www.aitech1.ru)

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+1V\_S5\_VCCF24  
2.7 K $\Omega$   
+/-1.0%



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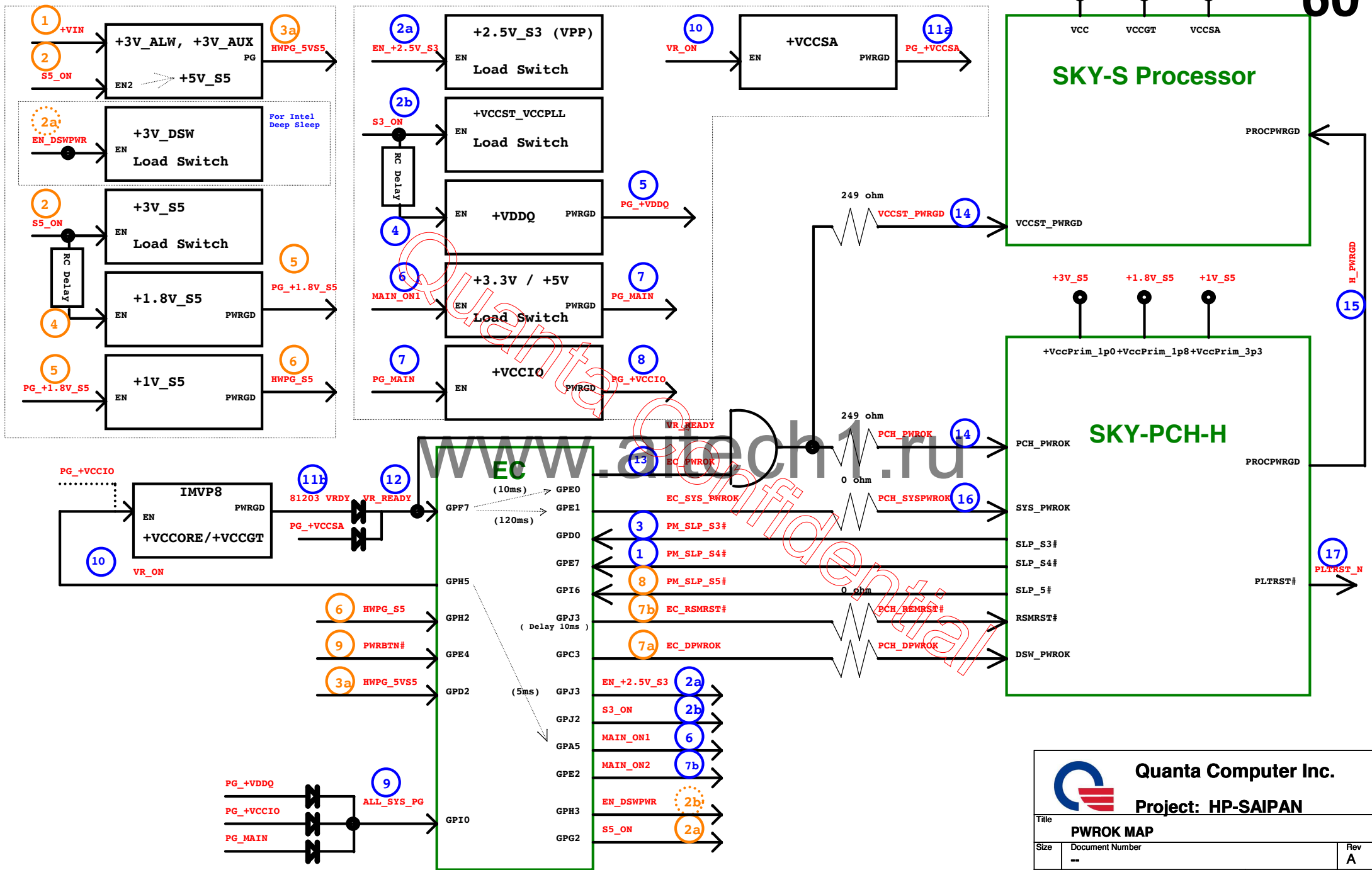
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Project: HP-Saipan

Title <b>CLOCK MAP</b>		
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# PWROK MAP / RSMRST\_PWRGD#





## DB1 Change List

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No.	Change details	Location/Description	Page	Change Reason
EC-DB1-E01	Change 0 ohm to shortpad	R76,R328,R329,R785,R166,R158,R732,R618,R351,R352,R358	5,9,10,12,16,26,34	Reduce 0 ohm usage for SMT.
EC-DB1-E02	Modify PEG HW straps	R489,R5106,R514	5	For PEG PCIe x4 Gen3 setting.
EC-DB1-E03	Remove AC caps on PEG [4:7] for N16S	C74,C73,C483,C479,C75,C76,C488,C497,C77,C78,C500	16	N16S-GMR support PEG x3 only.
EC-DB1-E04	Add dual mosfet on SMBI_CLK/DAT	C56,C73,C80,C567,C515	9	I2C power domain.
EC-DB1-E05	Remove C328	C328,C330	14,15	for DDR4 reset timing
EC-DB1-E06	Remove R612	R612	16	Don't support GC6.0
EC-DB1-E07	Remove R126,R118,R109	R126,R118,109	16,19	unnecessary
EC-DB1-E08	stuff R96	R96	9	NV suggest
EC-DB1-E09	De-populate SPI ROM	R64,R72,R129,U9,R124C102	19	De-populate SPI ROM
EC-DB1-E10	Change QHD panel circuit	all page	25	Chage QHD VCC control circuit
EC-DB1-E11	Chage R711 to 470 ohm	R711	25	QHD VCC discharge resistor
EC-DB1-E12	Change part	F9	26	common part
EC-DB1-E13	DMIC I2C circuit wrong	AR5/AR17/AR6/AR13	27	DMIC I2C circuit wrong
EC-DB1-E14	Change EC HW straps power domain to +3V_ALW	'--	30	timing issue
EC-DB1-E15	Stuff R571/R572	R571/R572	30	I2C power domain.
EC-DB1-E16	Remove R70	R70	30	Reduce 0 ohm usage for SMT.
EC-DB1-E17	Change +3.3V to +3.3V_CCD on CN4.1 & U3.5	CN4.1 & U3.5	31	To disable DMIC device in Fangio-x
EC-DB1-E18	Stuff U5,U4	U5,U4	31	ESD
EC-DB1-E19	Remove R3	R3	30	unnecessary


EC-DB-P01	change footprint to short pad.	PJP2,4-9,11-20,22-31	50-54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50-54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50-55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

## DB2 Change List

No.	Change details	Location/Description	Page	Change Reason
EC-DB2-E01	Change 0 ohm to shortpad	R552,R761,R735,R316,R307,R706,R164,R336	5,9,10,11,22,34	Reduce 0 ohm usage for SMT.
EC-DB2-E02	Adding TVS DIODE	R666,R306,R278,R324,136,R781,R667,R231,R703,R372	5,14,34	ESD request
EC-DB2-E03	Change location C378/C379 to FC329/FC330	D6,D7	6	power parts.
EC-DB2-E04	Remove R673	R673	11	simple circuit
EC-DB2-E05	Stuff C594 10pf	C594	11	for CK 24M-EC timing
EC-DB2-E06	Change Board ID to SI ( STUFF R702)	R702	12	BOARD ID
EC-DB2-E07	ADD TVS on WLAN_PCIE_CLKREQ#	D46	12	ESD request
EC-DB2-E08	Change part	L58	18	For common part
EC-DB2-E09	Chage C71 to 10pf and C72 to 12pf	C71,C72	18	Xtal accuracy
EC-DB2-E10	Don't stuff R18/R20	R18,R20	21	unnecessary
EC-DB2-E11	Don't stuff C116	C116	22	unnecessary
EC-DB2-E12	Don't stuff R181 and add R822 pull down	R181,R822	22	Reatek recommend
EC-DB2-E13	Chage caps power rating from 16v to 10v	C108,AC9	22	Change caps power rating
EC-DB2-E14	Chage C232 to and C228 to 8.2pf	C232/C228	24	Xtal accuracy
EC-DB2-E15	Change part	F9	26	For common part
EC-DB2-E16	Change Q10 to dual MOSFET. Q32/33 to Q57	Q10/Q11/Q10, Q32/Q33/Q57	26,34	Simple layout
EC-DB2-E17	Change part	AL9,AL10,AL11,AL13	27	For common part
EC-DB2-E18	adding disable DMIC icon	Aul.48	28	HP request
EC-DB2-E19	Stuff R803/R792/D33, don't stuff R802	R803,R802,R792,D33	12,28,29,34	enable PCIe clock request function
EC-DB2-E20	Adding M.2 SSD function	All page	35	HP request
EC-DB2-E21	Change RJ45 part	CN24	28	SMT request
EC-DB2-E22	Chage caps power rating from 10v to 6.3v	C230,C482,C495	29,34	Chage caps power rating
EC-DB2-E23	Stuff C666	C666	29	EMI request
EC-DB2-E24	Change GPIO table in EC	EN_TYPERC,CLR_CMOS,EN_AUDIO_PWD,BOX_BUTTON	30	common design
EC-DB2-E25	Change diode to 0 ohm	R837,R838,R839	30	common design
EC-DB2-E26	Change SMI circuit	R517	30	unnecessary
EC-DB2-E27	Adding IRMT control pin	R843	30	IRMT
EC-DB2-E28	Change QHD I2C control circuit	R627/R633	30	Leakage.
EC-DB2-E29	Remove D17/D19	D17/D19	30	unnecessary
EC-DB2-E30	Change L5 to 4.7ohm. Adding C674	L58,C674	31	DMIC EA timing
EC-DB2-E31	Stuff U5,U4	U5,U4	31	ESD
EC-DB2-E32	Add IRMT control circuit	R842,Q58,R840	31	IRMT
EC-DB2-E33	Reserve D45	D45	31	ESD
EC-DB2-E34	Change USB power switch	U43,U44,U33,U32,C342,C372	31,32	For common part
EC-DB2-E35	Change C235/C236 from 150uf to one 390uf (C236)	C235,C236	32	simple layout
EC-DB2-E36	Add M.2 SSD function	'--	35	HP request
EC-DB2-E37	Change Part	CN8	36	common design
EC-DB2-E38	Reserve C205	C205	36	Reserve only
EC-DB2-E39	Don't populate R384	R384	36	Leakage.
EC-DB2-E40	Remove LPC pin header	CN10	37	no enough layout space.

EC-DB-P01	change footprint to short pad.	PJP2,4-9,11-20,22-31	50-54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50-54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50-55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

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